Aviation and Defense

Edition 22
Sept. 2024




Welcome to the twenty-second edition of the Microchip Aviation and Defense Newsletter. We've provided products with a proven track record of innovation, quality and reliability to the aviation and defense community for more than 60 years.

We publish this newsletter quarterly with the goal of supplying you with the latest information on new product releases, qualification, test and documentation updates, the status of hardware kits and engineering samples, upcoming events and technical deep dives. A note to our readers: if you have a specific topic of interest, please email eli.kawam@microchip.com and we will do our best to address this topic.

With this edition, we continue the discussion of our Mission Assurance webinar series. You can watch season one (Oscillators and Timing) and season two (Power Tips and Tricks) by registering on our website.

Thank you for your support. Please feel free to forward this newsletter to your colleagues and friends who are interested in receiving important updates about our solutions.

Anyone can subscribe to receive future editions here.

Should you have questions or comments regarding this newsletter or have special topic requests, please feel free to contact me: Eli Kawam, Technical Marketing Manager, Microchip Technology, Aerospace and Defense Group at Eli.Kawam@microchip.com.

Our Mission Assurance webinar series provides deep technical dives into the technology, specification, reliability and performance of our products and solutions.

Season one contains 10 episodes that cover time and frequency topics such as basic quartz oscillators, VCXOs, TCXOs, OCXOs, SAW, MEMS and atomic clocks. The webinars cover all the technical details needed for space, aviation and defense applications including shock and vibration, temperature extremes and radiation effects.

Season two, titled “Case Studies in Power – Tips and Tricks”, consists of two episodes that address the technical details involved with the SG1524 PWM controller and the application of a Baker clamp to a driver circuit.

Watch seasons one and two on our website.

The original topic for season three, “Radiation and Its Effects on Semiconductors”, has been delayed until next year and will be replaced by “eVTOL Solutions”, which we plan to release at the end of 2024. Stay tuned.

Should you have any questions regarding this webinar series or if you would like to make a suggestion regarding future seasons, please contact Eli Kawam, Technical Marketing Manager, Aerospace and Defense Group at: eli.kawam@microchip.com.

Custom Reference Design: Microchip PolarFire® SoC Video Kit Integration

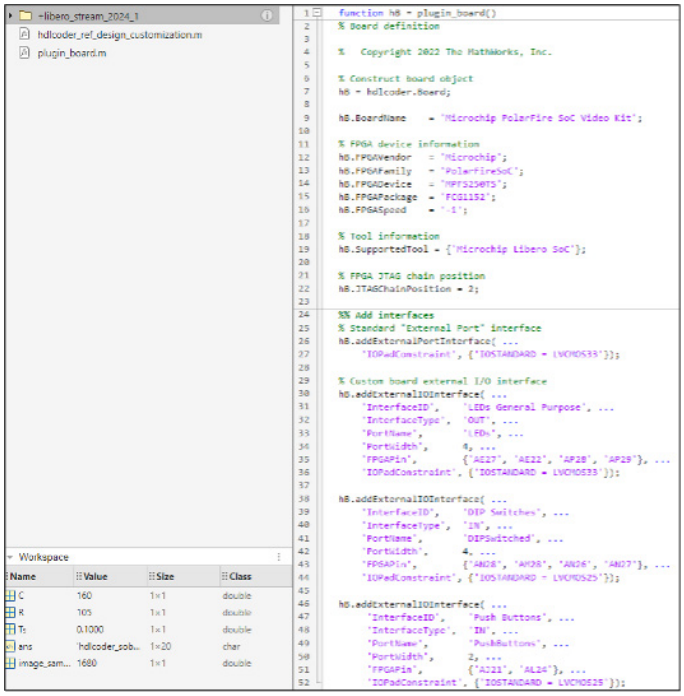
In the fourteenth edition of the Microchip Aviation and Defense Newsletter, we introduced the custom reference design workflow for the SmartFusion® 2 FPGA Advanced Development Kit with MATLAB® R2022A in HDL Workflow Advisor (HDLWA) with Libero® SoC Design Suite.

In this edition, we are delighted to introduce the integration custom reference design of PolarFire® SoC Video Kit along with all required IPs including HDMI_TX, HDMI_RX, Clock, Reset, XCVR Trans receivers and more with Libero SoC Design Suite.

You can now register the PolarFire SoC Video Kit and a custom reference design in the HDL Workflow Advisor for the Microchip workflow.

The reference design and custom board workflow with PolarFire SoC Video Kit for Libero SoC Design Suite can be executed in the following steps:

Step 1: Create board customization and reference design customization files for PolarFire SoC video kit.

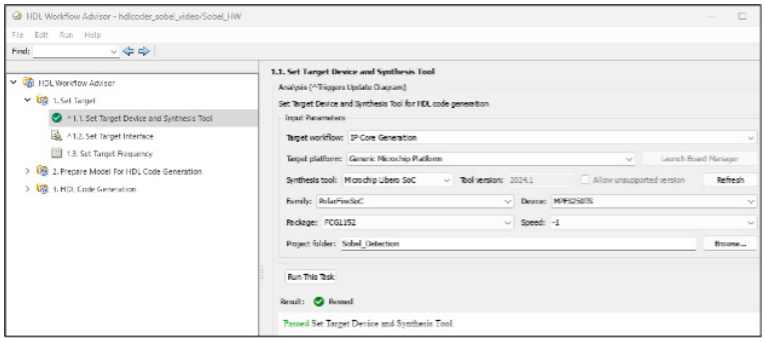


Step 2: Create custom block design TCL file from Libero SoC Design Suite and export it as TCL.

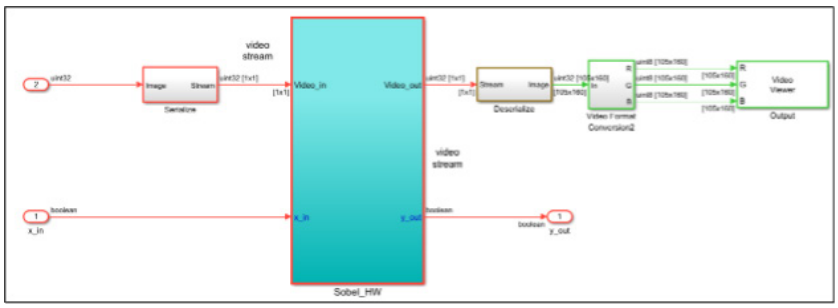
```
set install_loc [defvar_get -name ACTEL_SW_DIR]
set mss_config_loc "$install_loc/bin64/pfsoc_mss"
set local_dir [pwd]
set sd_name {Libero_sd}

#variable used in the design
set SimTime 100us
set Effort_Level true
set Repair_Min_Delay true
set Multi_Pass_Layout false

# Cores required to run the TCL script
set HDMI_TX_Version {5.2.0}
set PF_CCC_Version {2.2.220}
set PFSOC_INIT_MONITOR_Version {1.0.307}
set COREFIFO_Version {3.0.101}
set PF_TX_PLL_Version {2.0.304}
set HDMI_RX_Version {5.3.0}
set PF_XCVR_ERM_Version {3.1.205}
set PF_XCVR_REF_CLK_Version {1.0.103}


#tool profiles
set synprofile {Synplify Pro ME}

set simuprofile {QuestaSim ME}

#Device details
set family {PolarFireSoC}
set die_eval_SoC {MPFS250TS}
set eval_SoC_package {FCG1152}
set eval_Soc_part_range {IND}


############ Download Required Cores if not available ####################
download_core -vlnv {Actel:DirectCore:COREFIFO:3.0.101} -location {www.microchip-ip.com/repositories/DirectCore}
download_core -vlnv {Microsemi:SgCore:PFSOC_INIT_MONITOR:1.0.307} -location {www.microchip-ip.com/repositories/SgCore}
download_core -vlnv {Actel:SgCore:PF_CCC:2.2.220} -location {www.microchip-ip.com/repositories/SgCore}
download_core -vlnv {Microchip:SolutionCore:HDMI_TX:5.2.0} -location {www.microchip-ip.com/repositories/DirectCore}
download_core -vlnv {Microchip:SolutionCore:HDMI_RX:5.3.0} -location {www.microchip-ip.com/repositories/DirectCore}
download_core -vlnv {Actel:SgCore:PF_XCVR_REF_CLK:1.0.103} -location {www.microchip-ip.com/repositories/SgCore}
download_core -vlnv {Actel:SystemBuilder:PF_XCVR_ERM:3.1.205} -location {www.microchip-ip.com/repositories/SgCore}
download_core -vlnv {Actel:SgCore:PF_TX_PLL:2.0.304} -location {www.microchip-ip.com/repositories/SgCore}

# Import source files

import_files -hdl_source {HDMI_TX_Initiator_IF.v}
build_design_hierarchy

############ Create, configure and generate core components ##########################

#################### HDMI_TX_Initiator_IF ####################################
```

Step 3: Register PolarFire SoC video kit to HDL Workflow Advisor so that it will appear in target platform dropdown.

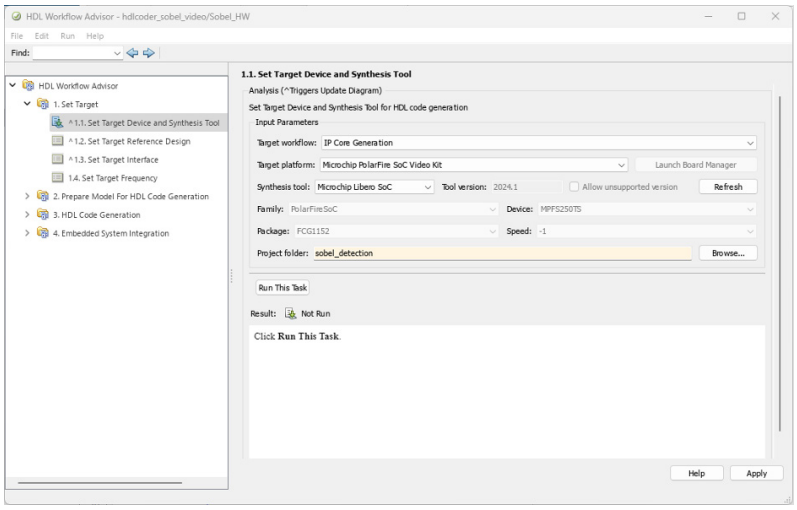
Step 4: Enable AXI4 stream interface for Libero SoC Design Suite and generate IP core for generic Microchip platform.



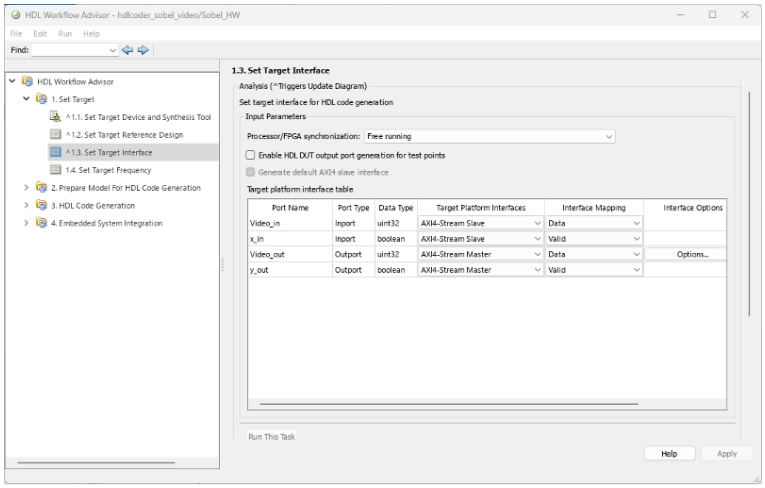
Step 5: Open hdlcoder_sobel_video.slx Simulink® model, which has edge detection algorithms inside Design Under Test (DUT).



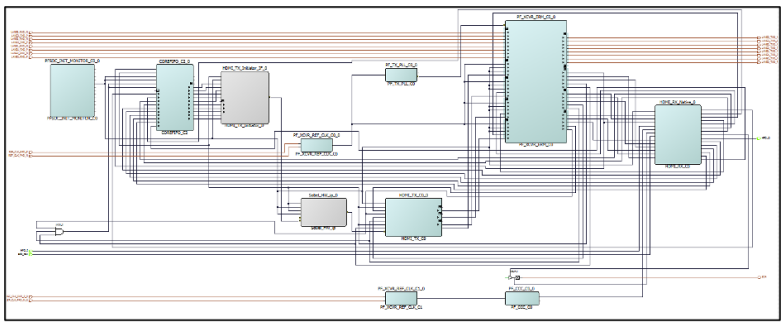
Step 6: Open HDL Workflow Advisor for DUT and set workflow as IP core generation and target platform as Microchip PolarFire SoC video kit.

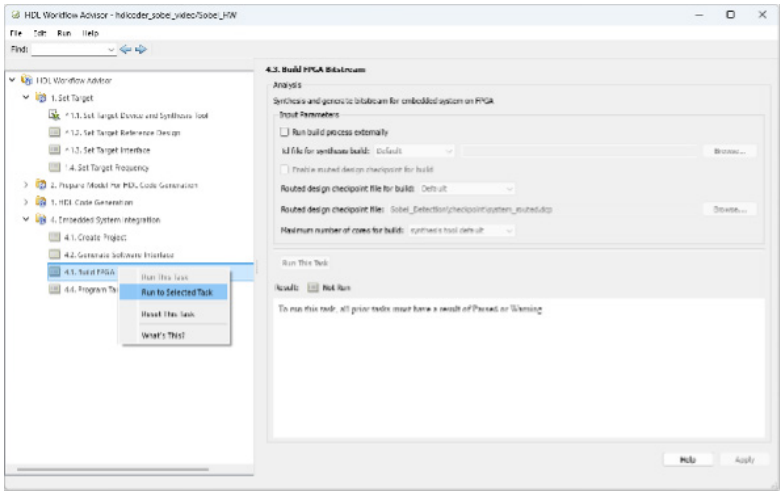


Step 7: Assign AXI4 stream master and AXI4 stream slave interfaces to input and output of DUT.

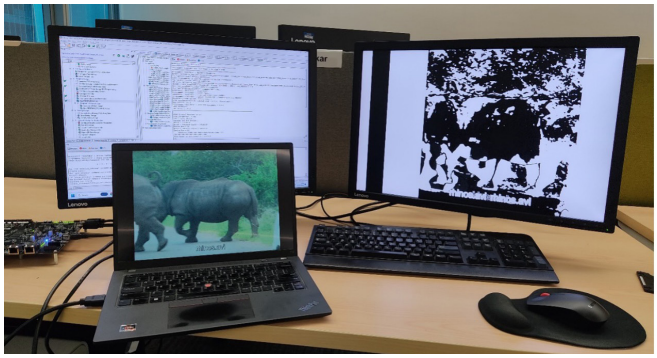


Step 8: Right click on task 4.3 (Build FPGA Bitstream) and click “Run to Selected Task” to generate bitstream.





Step 9: Connect video source to HDMI_RX input port of PolarFire SoC video kit through HDMI® cable. Connect HDMI_TX port of PolarFire SoC video kit to video viewer through HDMI cable to observe the output.



Required MathWorks® Tools

- MATLAB
- Simulink
- HDL Coder™
- HDL Verifier™
- Fixed-Point Designer™
- MATLAB Coder™
- Embedded Coder®

In addition to the software tools above, you will need the following hardware:

- PolarFire SoC Video Kit
- USB JTAG programming cable

The hardware support package automatically includes the PolarFire SoC video kit.

Once the tools are installed, you must set up the Libero SoC Design Suite tool path in MATLAB by invoking the “hdlsetuptoolpath” command from MATLAB prompt and set the path to Libero SoC Design Suite installer.

For additional information, please contact: Puneet.Kumar@microchip.com.

Application of Voltage-Controlled SAW Oscillators (VCSOs) in RADAR and Other Applications

By: Dan Porga, Senior Manager, SAW Products

Introduction

In analog-sensing applications, noise imposes a lower limit on the dynamic range that can be achieved. The most familiar form of noise in electronics is thermal noise, which arises from the random motion of charged carriers. Thermal noise is well understood and has a uniform power spectral density from DC to nearly a Terahertz that is commonly expressed in terms of dBm/Hz. Flicker noise is another important phenomenon important in electronic components and is characterized by a non-uniform power spectral density proportional to (1/F), where (uppercase) F here represents absolute frequency in Hz. At Radio Frequencies (RFs), the additive impact of flicker noise is usually unimportant, but it can be significant if it contributes to modulation.

In applications where the desired information is contained on a carrier, phase noise can be an important dynamic range limitation as well. When any carrier is phase modulated, either intentionally or inadvertently by noise (flicker, thermal or otherwise), sidebands are generated. Phase noise is commonly quantified as the power spectral density in one of those sidebands and is expressed in terms of dBc/Hz at a frequency offset of (lowercase) f Hz from the carrier. Phase noise is a frequency domain description and can be modeled as a power series of the term (1/f), as described in the seminal paper by D.B. Leeson [1]. It is strongest close to the carrier and drops off to the thermal noise floor at larger frequency offsets. Phase jitter is a quantification of the same phase noise phenomenon in the time domain. Jitter on a clock source driving an Analog-to-Digital Converter (ADC) or digital signal processing hardware will impact system performance.

An important example of this type of application is RADAR. Figure 1 illustrates a RADAR return spectrum comprised of two weak target signals in the presence of a strong clutter signal (e.g., the earth). Note: both sidebands are illustrated in the figure as would be observed on a spectrum analyzer. Presuming the targets and/or receiver are in motion, there will be a Doppler shift between the returns. If the receiver phase noise performance, which shows up as sidebands on the clutter signal (blue), is relatively large, the desired target (red) will be obscured. The other target, at 8 kHz Doppler shift (green), is observable even though it is the same level as the one at 2 kHz offset. Therefore, transmitting/receiving phase noise level directly impacts the probability of target detection and the frequency offset correlates to the target's radial velocity.

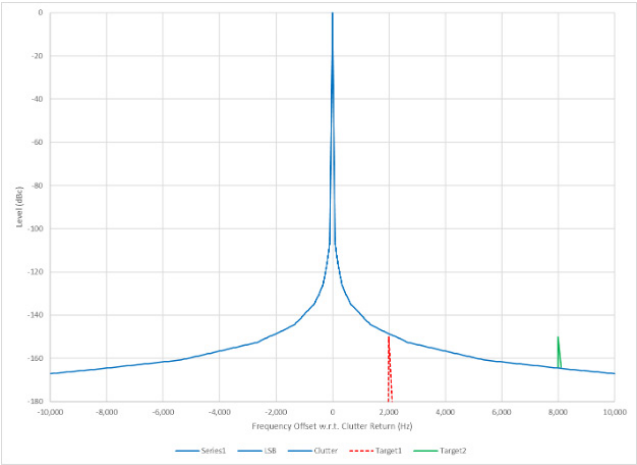


Figure 1: Example RADAR Return Spectrum

Voltage-Controlled SAW Oscillators (VCSOs), which will be described in this article, can offer significant advantages to system phase noise performance in the frequency offset range of 1 kHz to 1 MHz. In a RADAR system, these frequency offsets correspond to radial velocities ranging from those of ground vehicles to hypersonic missiles.

VCSO Implementation

A block diagram of a VCSO is shown in Figure 2. Barkhausen's criteria establish the necessary conditions for oscillation: a feedback loop exists, positive gain exists and the loop phase is an integer multiple of 360 degrees. The last condition is desired at only one frequency and thus a frequency-selective element, typically a resonant device, is used in the feedback loop. There is a wide variety of technologies that could be used to implement the resonant device; in the case of a VCSO, a Surface Acoustic Wave (SAW) resonator is used.

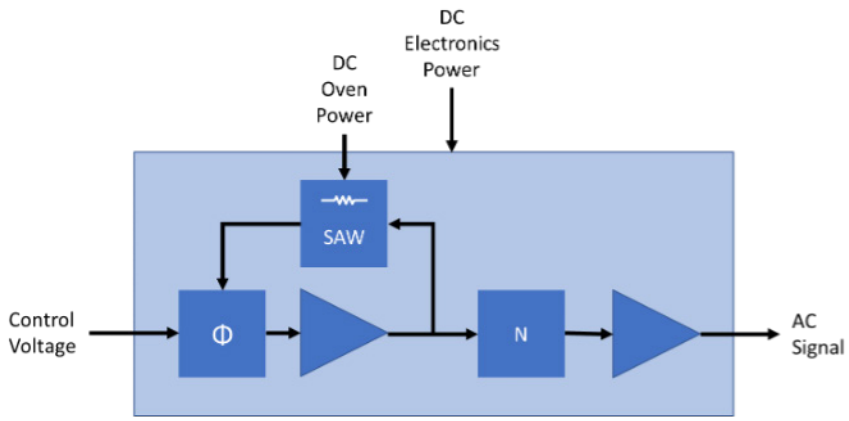


Figure 2: Block Diagram of a Voltage-Controlled Oscillator

SAW devices exploit the piezoelectric effect exhibited by certain materials, which couples mechanical strain with electric field. Structures are photolithographically printed on the surface of a piezoelectric substrate that consists of periodically spaced metal electrodes. Figure 3 illustrates a device containing two Inter-Digital Transducer (IDT) structures. In a transducer, two groups of electrodes are formed by connecting each group with a common bus. When a potential is applied across the bus bars, an electric field is induced between electrodes of opposite polarity which, in turn, produces a mechanical strain at these locations. When the fields are time varying, many types of acoustic (mechanical) waves are generated in the substrate at each strained location and radiate away. SAW devices are designed to preferentially generate waves that are tightly bound to the surface of the substrate; hence, their name. The most familiar experience of surface waves is ripples on the surface of water; however, for the commonly used SAW Rayleigh mode, the wave behavior is more akin to that of an earthquake. The fact that these acoustic waves propagate 100,000 times slower than electromagnetic waves make them extremely useful for the design of highly miniaturized filter and resonator devices.

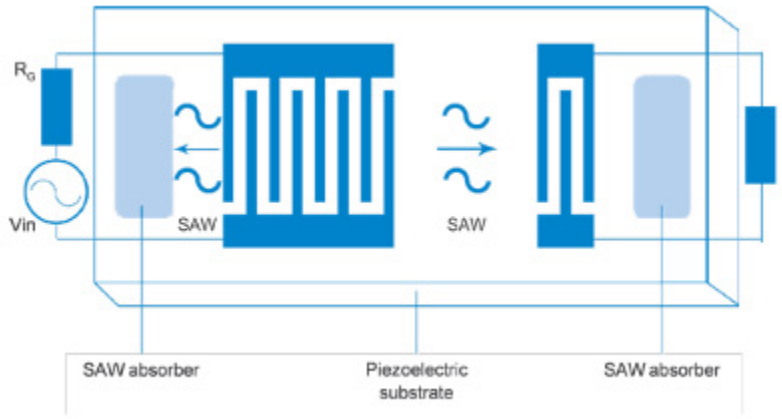


Figure 3: SAW Device Comprised of Two Transducers

A SAW resonator is constructed by placing one or more transducers between mechanical reflecting structures to form a resonant cavity. The transducer behavior is reciprocal, meaning they can both generate and detect acoustic waves. The reflecting structure is formed by a periodic grating of electrodes, similar to the transducers, but electrically isolated from them. The resonant frequency of the entire device is inversely proportional to the spacing of the periodic electrodes and is largely controlled by the photolithography process. The frequency range practical for SAW technology is approximately 30–3,000 MHz, though the useful range for SAW resonator devices specifically is narrower. Note that all of the desired behavior is occurring at the surface of the substrate. This provides both a great degree of design flexibility and the opportunity to distribute the input power over a wide area, which is beneficial with regards to power density and, hence, long-term stable performance of the device.

An example of the phase noise performance achievable with a VCSO is presented in Figure 4 below.

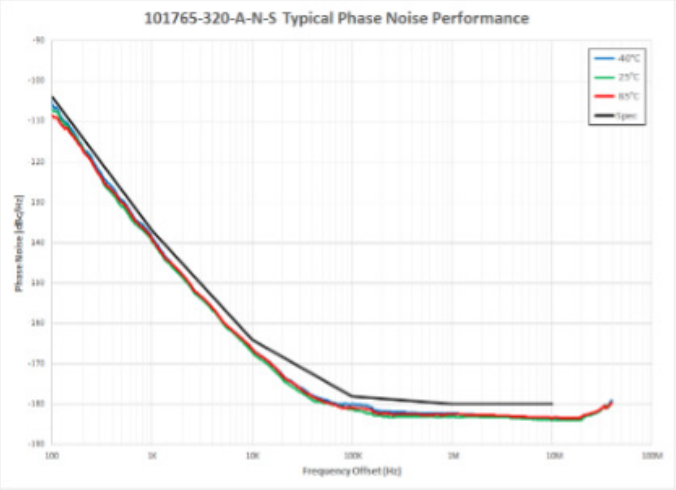


Figure 4: Example VCSO Phase Noise Performance at 320 MHz (Microchip Model 101765-320-A)

Comparison of VCSOs to Oscillators Based on Crystal Resonators (XOs)

As mentioned above, a wide variety of resonant structures can be used to build oscillators. At RF, oscillators constructed with crystal resonators (e.g., VCXOs, TCXOs and OCXOs) are common. These resonators also employ the piezoelectric effect but are based on acoustic waves that propagate in the bulk of the "substrate" rather than on the surface. The reflecting structures are the free surface boundaries at the top and bottom side of the crystal and the resonant frequency is inversely proportional to the thickness of the crystal. The resonant frequency is largely controlled by altering the physical dimensions of the crystal (e.g., grinding and lapping) and frequencies between 10 MHz and 100 MHz are commonly available. As the desired resonant frequency increases, the crystal becomes thinner and its power handling ability and mechanical stability diminish. Decreased resonator drive level in turn limits the phase noise performance achievable at larger frequency offsets relative to the carrier. An example of the phase noise performance achievable with an OCXO is presented in Figure 6 below (yellow curve).

If the desired operating frequency is higher than can be practically implemented with an XO, an easy solution would be to use a non-linear device, such as a frequency doubler, to generate a strong harmonic of the XO output. This does result in the desired "multiplication" of the XO frequency but comes with a penalty of degraded phase noise performance; the ideal degradation is 20*log (M) dB where M is the multiplication factor. The crystal resonator's Q factor (which impacts the XO phase noise in the flicker region), is so good that this degradation, particularly at low offset frequencies, is typically acceptable. In addition, cascading the multiplied XO output with a filter can be effective at cleaning up the degraded phase noise at high offsets; however, design constraints, including temperature effects, impose challenges filtering the middle range of offset frequencies. If phase noise at offsets between about 1 kHz and 1 MHz is an important or critical system consideration, a better solution is to phase lock a VCSO to the XO.

Phase Locked Loop Architecture

A block diagram depicting a VCSO and an XO in a Phase Locked Loop (PLL) architecture is shown in Figure 5. This architecture implements a feedback loop that forces the phase of the VCSO to be coherent with the phase of the XO. While it is not explicitly shown in the diagram, the PLL block includes a frequency divider circuit to bring the nominal VCSO output frequency down to that of the XO, a phase detector circuit that compares the divided VCSO waveform to the XO waveform and a loop filter. The PLL block output is proportional to the phase difference between the two and drives the VCSO control voltage input to make them equal.

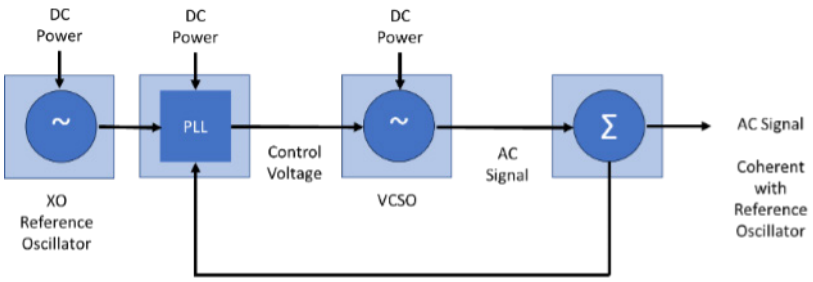


Figure 5: Block Diagram of PLL Architecture

Inside the PLL bandwidth, the overall performance will follow the XO performance (as if it were multiplied to the output frequency); otherwise, it will follow the VCSO performance. What that means is that the overall performance reflects the best of both the XO and the VCSO capabilities: the stability and close-in phase noise of the XO and the higher output frequency and phase noise at larger offsets of the VCSO. This situation is illustrated in figure 6 where the PLL (orange) curve represents the overall output. In this idealized example, the PLL bandwidth is 750 Hz.

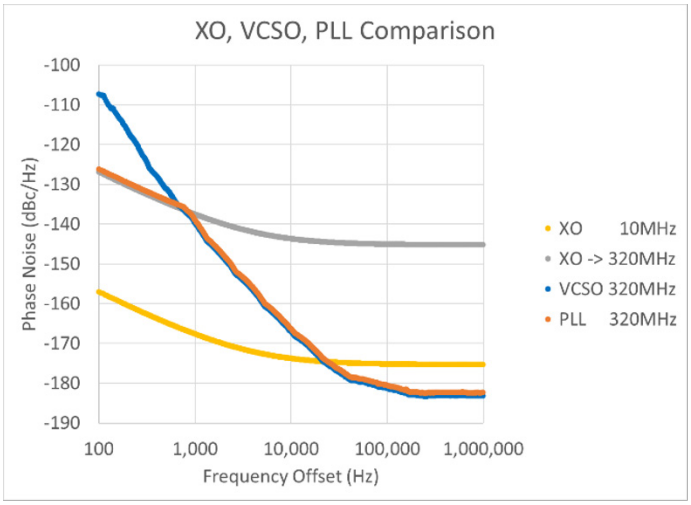


Figure 6: PLL Performance Illustration (Microchip Models OX-204 and 101765-320-A)

Conclusion

In this article, we have reviewed how phase noise impacts a RADAR system's performance and a means to improve it using a VCSO in a PLL architecture. The use of multiple VCSOs can offer further improvement based on the uncorrelated nature of the noise in each individual VCSO. The phase noise improvement available with this approach is 10*log(N), where N is the number of VCSOs used. Note that if the VCSOs are phase locked to a common XO, the noise improvement will only be realized outside of the PLL bandwidth. The Size, Weight and Power (SWaP) and cost of VCSOs makes this a practical option if the required system performance dictates it. This is particularly true of an Actively Electronically Steered Array (AESA) RADAR architecture that is naturally broken down into multiple sub-arrays, each of which could be driven by its own VCSO.

While the examples discussed have pertained to RADAR applications, the phase noise benefit of VCSOs can also be applicable in other sensing applications or anywhere a clock is required to drive an ADC or digital signal processing hardware.

[1] D. Leeson, „A simple model of feedback oscillator noise spectrum," Proceedings of the IEEE, 1966.

Should you have questions or comments regarding this newsletter or have special topic requests, please feel free to contact me: Mike Ziehl, Sr. Marketing Manager, Discrete Products Group at Mike.Ziehl@microchip.com

FPGA Discovery kit: A Low-Cost Evaluation Board

The embedded industry is witnessing increased demand for open-source, RISC-V®-based processor architectures, but there are limited options in commercially available silicon or hardware.

Our full-featured, low-cost PolarFire SoC Discovery Kit enables rapid testing of application concepts, development of firmware applications and programming and debugging for designs using RISC-V-based FPGAs. This ready-to-use development platform is an excellent option for students, new and experienced designers and the open-source community.

PolarFire SoC is our latest generation of FPGA with four RISC-V application cores. This System on Chip (SoC) is well suited for low-power, highly reliable embedded processing. The SEU configuration immunity makes it a great choice for defense and aviation applications. PolarFire SoC delivers a CoreMark® score of 6500 at 1.3W, giving it a distinct advantage over other SoC FPGAs in the market. PolarFire SoC also features defense-grade security and best-in-class anti-tamper countermeasures.

PolarFire SoC Discovery Kit

The Discovery Kit is based on the MPFS095T-1FCSG325E PolarFire SoC. It offers 93K logic elements and an embedded microprocessor (MPU) subsystem that includes a quad core and a 64-bit CPU cluster based on the RISC-V Instruction Set Architecture (ISA). A large L2 memory subsystem can be configured for performance or deterministic operation and supports Asymmetric Multi-Processing (AMP) mode. The kit comes with expansion capabilities, including a Raspberry Pi® interface connector to add Hardware Attached on Top (HATs), a mikroBUS™ connector to connect with Click boards™ and a seven-segment display connector to support a seven-segment, eight-digit board. It also has a Raspberry Pi MIPI® RX connector for interfacing with the MIPI CSI-2® camera module. Visit the product page to learn more about our PolarFire SoC Discovery Kit.

The Discovery Kit also includes support for the Mi-V ecosystem, which offers a comprehensive suite of design tools, OS/RTOS, solutions, design services, hardware and IPs/CPUs. This ecosystem is continuously expanding and today we have close to 80 partners. Learn more about the Mi-V RISC-V ecosystem.

For any questions or comments regarding this newsletter, please feel free to contact Tom Wright, Senior Marketing Manager – FPGA, at tom.wright@microchip.com

Overview Of LX4580 Serial Interfaces and Bus Error Management

This is the sixth in a series discussing topics around LX4580 implementations. The LX4580 is an analog front-end for high-reliability motor-actuator control systems working under stringent standards such as DO-160 for avionics in airborne systems. The LX4580 interfaces with dual MCUs or FPGAs in redundant COM/MON system architectures and features ECC encoding to provide 1-bit error correction and 2-bit error detection. Sequential logic is implemented with Triple Mode Redundancy (TMR) to protect against Single-Event Upsets (SEUs).

The block diagram below shows a typical PMSM motor-actuator system using redundant LVDTs for actuator linear position feedback. The LX4580 combines analog sensor acquisition and motor control PWM synthesis. Motor current sensing and LVDT secondary waveform acquisition uses a dedicated Σ-Δ ADC per channel, nine in total. The LX4580 also includes sensor interfaces, which use a state machine and a pair of 10-bit SAR ADCs for digitization. The topic of this article is to provide an overview of the dual serial interfaces which interface the internal registers and discuss the error-detecting and correcting architecture. These blocks are shown in pink in the block diagram.

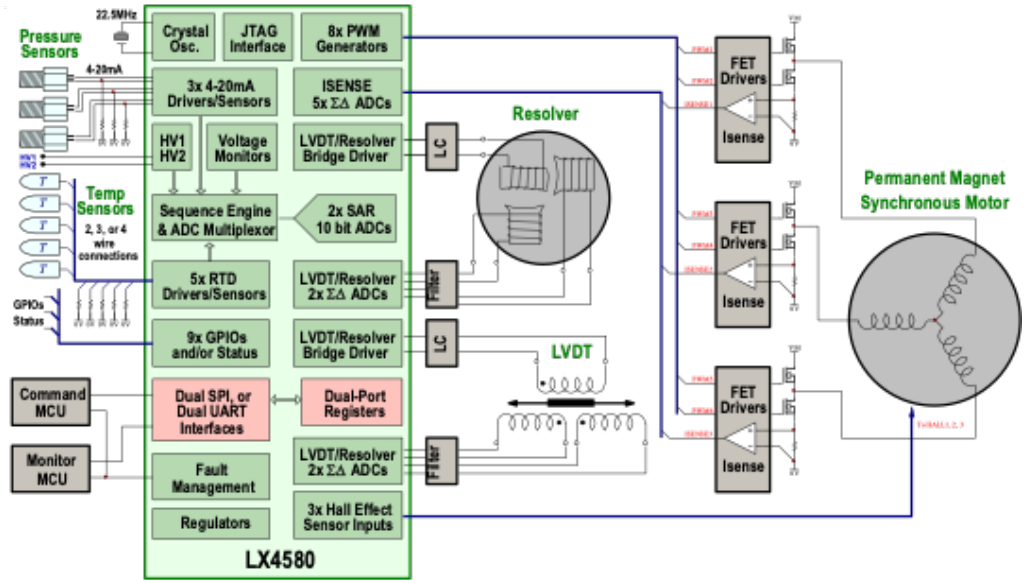


Figure 1: Typical PMSM System

The LX4580 offers two serial interfaces, each with simultaneous and asynchronous dual-port read/write access to the register set. The dual interfaces allow the control system to implement a classic COM/MON architecture. This implements a main (command) processor to operate an actuator, while a second (monitor) processor examines the same measurement data to double-check the command processor's actions. A bus between the two processors shares measurement and control data for comparison.

The LX4580's serial interfaces are selected by a pin to be both either asynchronous (using two pins: TXD and RXD) or synchronous SPI (using four pins: SS, CLK, MOSI and MISO). The SPI interfaces are fast, up to 30 MHz, and generally preferable. The asynchronous alternative is limited to 1 MHz but is operated more easily over long wiring harnesses since there is no timing relationship between the bus lines.

A single command from a serial interface host to a LX4580 consists of four 16-bit SPI packets. For the asynchronous interface option, each 16-bit packet is further split into two 8-bit chunks (plus start, parity and stop bits). Each 16-bit packet comprises 11 payload bits and five parity bits as a Hamming 16-11 Error Correction Code (ECC) implementation. This Hamming code is Single-Error Correcting and Double-Error Detecting (SECDED) due to the inclusion of the fifth parity bit. This means that for every 16-bit communication, a single bit error is guaranteed to be detected and corrected, and so the data will be used. If the 16-bit packet has two flipped bits, the packet won't be corrected, but the transmission error will be detected. In this case, the uncorrectable packet is ignored. In either case, the LX4580's FAULT pin alerts the host, and an internal register identifies the issue.

It's worth comparing the LX4580's Hamming code with conventional parity error detection. Single-bit parity adds an extra bit to a packet (so a 16-bit word would become 17 bits) to indicate whether there are an even or odd number of ones in the packet. It guarantees the detection of a single-bit error anywhere in the packet (including the parity bit), but doesn't identify the bit. This provides single-bit error detection, but not correction. Unfortunately, single-bit parity guarantees not to detect a packet with any two bits at fault. This is because two flipped bits have the same parity as no flipped bits. Single-bit parity is useful where single bit errors are rare, multiple bit errors very rare and also when data integrity is not especially critical (such as a printer output). As a

further note, single-bit parity actually guarantees to detect any odd numbers of bit errors (1, 3, 5…), but will not detect any even numbers of bit errors (2, 4, 6…).

The fundamental four-packet structure for LX4580 register write access is shown in Figure 2 below. The first bit of every packet is 0, indicating that the packet is from the host. The next two bits are Packet ID bits, which identify which of the four types of packets it is. The next eight bits are the packet's payload, which includes Command {C0:C3}, 12-bit register address {A0:A11} and 16-bit register data {D0:D15}. The final five bits are parity of each packet are Hamming parity bits {P0:P4}.

Figure 2: Four-Packet Serial Interface Transmission From Host to LX4580 (Register-Write)

Packet	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
	0	Packet ID									Parity					
First Command {C0:C3} Address {A0:A3}	0	0	0	C0	C1	C2	C3	A0	A1	A2	A3	P0	P1	P2	P3	P4
Second Address {A4:A11}	0	1	0	A4	A5	A6	A7	A8	A9	A10	A11	P0	P1	P2	P3	P4
Third Data {D0:D7}	0	0	1	D0	D1	D2	D3	D4	D5	D6	D7	P0	P1	P2	P3	P4
Last Data {D8:D15}	0	1	1	D8	D9	D10	D11	D12	D13	D14	D15	P0	P1	P2	P3	P4

For LX4580 register read access, the last two packets are data read from the LX4580, as shown in Figure 3 below. Each packet contains 10 data bits as opposed to just a byte, which allows the results of the LX4580's 10-bit ADCs, for example, to be read in one packet.

Figure 3: Final Two Packets Transmitted From LX4580 to Host for Register-Read

Packet	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
	Data Ready											Parity				
3rd Data D8-D9,{D0:D7}	1	D8	D9	D0	D1	D2	D3	D4	D5	D6	D7	P0	P1	P2	P3	P4
Last Data {D6:D15}	1	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	P0	P1	P2	P3	P4

The four-bit command nibble is the key to optimizing efficient use of the serial interface, reducing register addressing overhead and unnecessary data transfers to a minimum. The four bits select register access options as follows:

- Read or write just the lower byte of a register in a three-packet transaction
- Read or write just the upper byte of a register in a three-packet transaction
- Read or write both the lower byte and the upper byte of a register in a four-packet transaction
- Read or write just the lower byte of sequential registers in a three-packet transaction for the first register, plus a single packet for subsequent registers (address auto-incrementing)
- Read or write just the upper byte of sequential registers in a three-packet transaction for the first register, plus a single packet for subsequent registers (address auto-incrementing)
- Read or write both the lower byte and the upper byte of a register in a four-packet transaction for the first register, plus two packets for subsequent registers (address auto-incrementing)

The optional byte or word access avoids unnecessary data, while the address auto-incrementing allows a bank of data to be accessed with the minimum overhead of just sending the initial address. In systems that don't need dual processor access to an LX4580, both buses could be used by a single processor. This allows one code section to be interrupt based using one bus without concern for the main code body using the other bus asynchronously.

The LX4580 is sampling now with an evaluation board also available. Product information can be found on the LX4580 web page. For additional information, please contact Dorian Johnson, Product Marketing Manager for Mixed-Signal Aerospace Products, at Dorian.Johnson@microchip.com

Aircraft Lightning Protection for ARINC and AFDX Protocols

By Kent Walters

Threat and Environment

It is common for lightning to strike jet airliners. It occurs about once every 1,000 flying hours while passengers and crew are safely transported to their destinations. Fly-by-wire systems failures at data signal interfaces are unacceptable. Surge protection at thousands of signal line interfaces provides reliable continuous performance from voltage spike damage using the designer's choice of silicon Transient Voltage Suppressor (TVS) devices.

There are two Aircraft Radio Inc. (ARINC) standards for signal protocols used for virtually everything that flies with "fly-by-wire" controls involving ARINC 429 as well as ARINC 664 or what is also identified as Avionics Full Duplex Switched Ethernet (AFDX). They are used to transfer critical data including air speed, temperatures, tire pressure, center of gravity, fuel weight, engine performance, external control surfaces and a host of other information. Interconnections are twisted, shielded line pairs for reduction of noise and induced lightning transients. For ARINC 429, there are two data transmission speeds, 12.5 kbit/s (low-speed) and 100 kbit/s (high-speed), with operating voltages typically ranging from +/- 5V up through +/- 17V. The latest ARINC 664 has notable improvements including Ethernet speeds up to a maximum of 100 Mbit/s or 1000 times faster than high-speed ARINC 429.

TVS types for these applications typically include bi-directional 500W Peak Pulse Power (PPP) ratings @ 10/1000 ms or more, such as the MSMBJ5.0CA series for slow data rates and the low capacitance MSMBJSAC5.0 types for 100 kbit/s data rates. The 1500 W rated MSMCJ5.0 and MSMCJLCE low-capacitance series are similarly required on more severe lightning threats defined in RTCA/DO-160G, Table 22-2 for pin injection. These low-capacitance TVSs are now complemented by "ultra-low capacitance" TVSs for the faster ARINC 664 Ethernet protocol included in Table 1 below.

Silicon p-n junction TVS devices typically have the same Peak Pulse Power (PPP) rating in a product series as shown in many TVS data sheets for the voltage range they cover. For example, when the voltage is doubled, the surge current rating (IPP) is reduced by half. For higher IPP or signal voltages, the 1.5 kW devices may be required for protection or by the severity of waveform and threat levels (see MicroNote 132). Table 1 below exemplifies the lowest voltage in the TVS series shown.

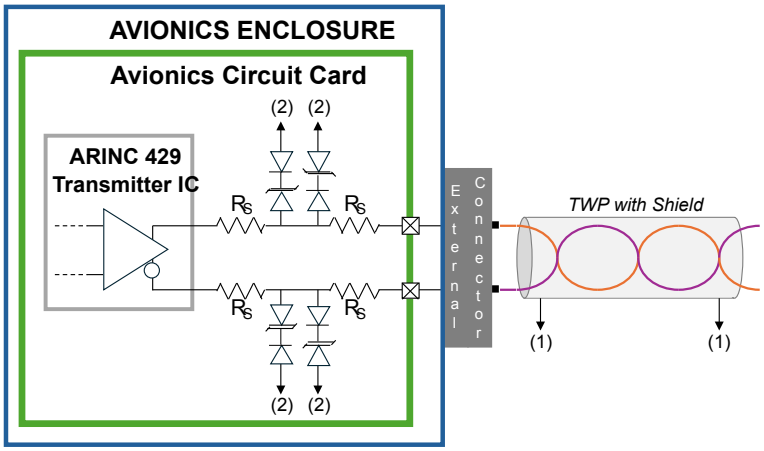
The following sections guide the designer in selecting optimum suppressor devices.

Table 1: ARINC TVS Selection Matrix

IPP Exposure levels	For 12 kbit/s Data Rate (ARINC 429 Low-Speed)	For 100 kbit/s Data Rate (ARINC 429 High-Speed)	For 100 Mbit/s Data Rate (ARINC 664)
Low	MSMBJ5.0CA Series PPP rating 500 W	MSMBJSAC5.0 Series PPP rating 500 W	1N8183 series PPP rating 500 W
High	MSMCJ5.0CA Series PPP rating 1500 W	MSMCJLCE6.5 Series PPP rating 1500 W	1N8221 series PPP rating 1500 W

An example ARINC line driver at one end of a data bus is shown in Figure 1 where the same TVS protection would also occur at the opposite end of the data bus. This will also be further discussed for faster ARINC 664 speeds. Depending on ARINC speed requirements, the choice in low capacitance TVS will vary as shown above in Table 1.

Figure 1: Protected High-Speed Line Driver



LEGEND

RS Series resistors for current limiting and impedance matching. See manufacturer's recommended values.

TVS Microchip Transient Voltage Suppressor

(1) Connect to aircraft frame ground

(2) Connect to avionics internal ground

NOTE: Some transmitter ICs have internal series resistors. If so, that resistance adds to RS in Equations 2, 4 and 8.

Aircraft Transient Waveforms

The conventional 10/1000 ms test waveform ("double exponential") at which most silicon TVSs are specified was earlier derived from a Bell Lab specification published in the late 1960s before other standards were developed. Since that time, we have seen a host of others including those defined by the aircraft industry as described in RTCA/DO-160G.

Section 22, Table 22-2 of this document accurately defines threat levels, including open circuit voltage and short circuit current plus six waveforms ranging from 5 ms up through 500 ms. Pin surge levels are listed in a matrix of fifteen separate pin injections threats as shown below.

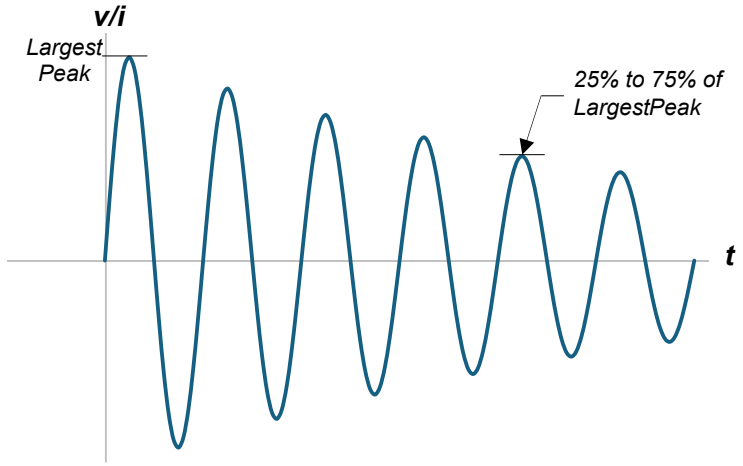
Table 2: Pin Injection Levels From RTCA/DO-160G Table 22-2

Level	Waveforms		
	3	4	5A
	Voc/Isc	Voc/Isc	Voc/Isc
1	100/4	50/10	50/50
2	250/10	125/25	125/125
3	600/24	300/60	300/300
4	1500/60	750/150	750/750
5	3200/128	1600/320	1600/1600
ZS	25 Ohms	5 Ohms	1 Ohm

The most common specified injection threat levels for data lines include waveforms 3 and 4 and normally at Level 3 or Level 4 at worst case. The source resistance ZS can be determined with the Voc/Isc quotient values.

Waveforms are shown below in Figures 2 and 3:

Figure 2: Voltage/Current Waveform 3



Note: Frequency for pin injection test is applied at 1.0 MHz (±20%). Voltage and current are not necessarily in phase.

Figure 3: Voltage Waveform 4

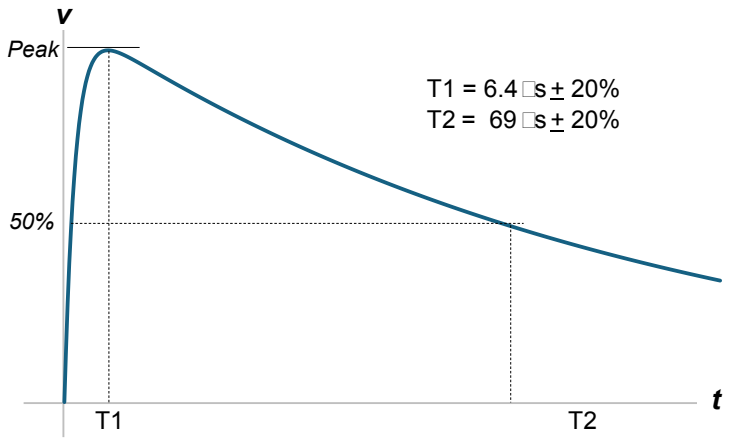
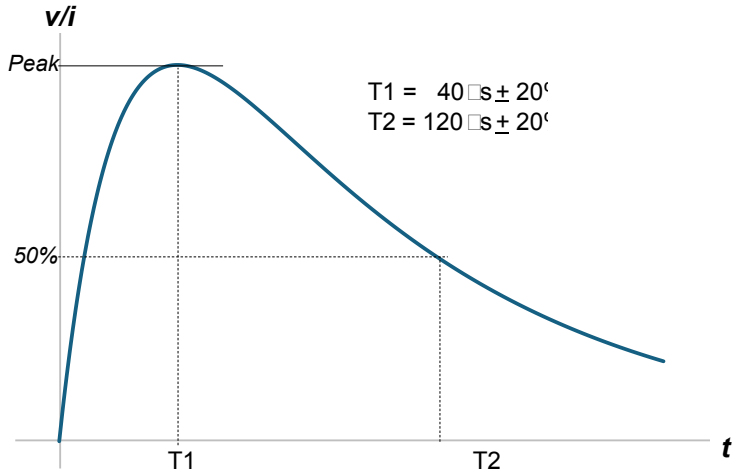


Figure 4: Voltage Waveform 5A

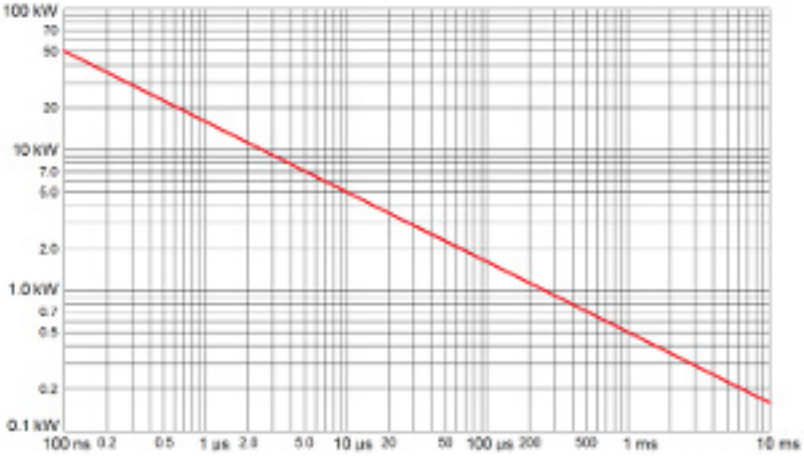


Calculating IPP Capability

Let's work out an example for protecting a slow data rate line, 12.5 kbit/s per ARINC 429, initially selecting an SMBJ5.0C for this application. What is its capability for protecting from a surge at Level 3, Waveforms 3 and 4 in Table 22-2 for Pin Injection in RTCA/DO-160? First, we translate the maximum TVS peak pulse current (Ipp) rating at 10/1000 ms into its equivalent for Waveform 3.

We need to refer to an example PPP and IPP versus time graph that also references the 10/1000 ms waveform below:

Figure 5: PPP vs Time for Low-Capacitance SMBJSACxxx Series (PPP Rating 500 W @ 10/1000 µs)



tW: Pulse Width to 50% Decay Point

Waveform 3 is equivalent to 5 ms exponential decay and applied frequency of 1.0 MHz (±20%) for each leg of a bi-directional low-capacitance TVS in Figure 1. To calculate the equivalent current capability of the SMBJSAC5.0 rated at 44 Amps @ 10/1000 µs, use the following method:

Equation 1:

IPP @ 5 ms = (Ppp @ 5 ms / Ppp @ 1000 ms) × Ipp of SMBJSAC5.0 @10/1000 ms

= (7000 W / 500 W) × 44.0 A, where the values of 7000 W and 500 W are from Figure 5 above

= 14 × 44.0 A

= 616 A

We shall be conservative and use a multiplication factor for the short Waveform 3 of 11.3 times IPP at 10/1000 ms, also shown in MicroNote 127 Table 2. This results in IP = 11.3 × 44.0 = 497 Amp capability well beyond that needed for Waveform 3, calculated as only 23.6 A in a similar manner as Eq 3 for the more severe Waveform 4 using a source resistance (ZS) of 25 ohms in Table 2.

For a much longer 69 ms pulse in Waveform 4 with tolerance +/- 20 %, we use the worst-case high side of 83 µs.

Equation 2:

IPP @ 83 ms = (1500 W / 500 W) × 44 A (IPP for SMBJSAC5.0)

= 3.3 × 44 A = 145 A

The multiplication factor of 3.3 for IPP is for the shorter 83 µs on Waveform 4 compared to 10/1000 µs in Figure 5, as also shown in MicroNote 127 Table 2.

It should be noted that the multiplication factors of 11.3 and 3.3 in the equations above also apply to TVS devices with other PPP ratings as shown in MicroNote 127 Table 2. The 5 ms pulse approximation for Waveform 3 may vary from one chart to another, but this is a non-issue since silicon TVSs are very conservatively rated for short pulse widths. From Table 22-2 in the RTCA/DO-160 specification, one can observe that this device will easily perform at Levels 3 and 4 for Waveforms 3 and 4 under worst-case conditions.

Calculating Requirements for the TVS

In the section above, we used the important PPP vs pulse width features of TVS devices or what is often identified as a Wunsch-Bell curve. That performance curve also represents the same elevated junction temperature during the transient event before failure occurs if driven well beyond that. From this curve, we calculated the equivalent IPP for shorter pulse widths of 5 ms and 83 ms for specific device types. The VC changes very little along the Wunsch-Bell curve as PPP and IPP capabilities increase with shorter pulse widths since most of the increase in voltage above the low current VBR is from the positive temperature coefficient of VC.,also described in MicroNote 125.

In this section, we will calculate the incident pulse current threat for a specified RTCA/DO-160G threat level, factoring in the influence of the TVS voltage selection for Working Standoff Voltage (VWM) and its VC .

In Level 4, Waveform 4, the incident pulse threat is specified as a 750V open circuit voltage with a 150A short circuit current. The operating voltage example is +/- 12 V. Do we need an SMBJ12CA or a higher current **SMCJ12CA** TVS of device?

First, calculate source impedance, Zs, using the values of Voc and Isc in Table 2-22.

Equation 3:

Z = Voc/ Isc

= 750 V / 150 A

= 5 ohms

When including clamping voltage (VC) effects for Waveform 4, the **peak impulse current (IPP)** threat is:

Equation 4:

IPP = (Voc – Vc) / Zs (where Vc is device max clamping voltage)

= (750 V – 19.9V) / 5 ohm (19.9 V is the VC of the SMBJ12CA or SMCJ12CA)

= 146 A

This same method of calculation is also further described in MicroNote 125

Using our multiplication factor of 3.3 for Waveform 4 calculated in equation 2 above:

Equation 5:

SMBJ12CA capability is 30.2 A (10/1000 ms) × 3.3 = 101A (6.4/83 ms)

Equation 6:

SMCJ12CA capability is 75.3 A (10/1000 ms) × 3.3 = 251A (6.4/83 ms)

Having an IPP rating of 101 A, the SMBJ12CA is insufficiently rated for this hypothetical application, leaving the SMCJ12CA as is the only option for Level 4, Waveform 4. It is unnecessary to calculate for Waveform 3 since its threat is inherently well below the threat level of Waveform 4.

As stated earlier in this article, most transient voltages across signal lines have attenuation levels above the source impedance that is added by series resistors for circuit impedance matching in the signal loop.

For an additional exercise, what would be the performance level for an HSMBJSAC5.0 with ARINC 429 and data rates of 100 kbit/s under threat conditions of Level 3, Waveforms 3 and 4? Again, we only need to determine the current for Waveform 4, which has Voc and Isc values of 300V and 60A, respectively.

Equation 7:

Zs = 300V / 60A = 5 ohms

Equation 8:

IPP = (Voc – Vc) / Zs

= (300V – 10V) / 5 ohms

= 58A for 6.9/83 ms pulse

The MSMBJSAC5.0 has an IPP of 44A @ 10/1000 ms. For 6.9/83 ms IPP is:

Equation 9:

IPP = 44A × 3.3 = 145.2 A for a 6.9/83 ms pulse

Here we observe that the HSMBSAC5.0 is capable of withstanding a 145A pulse for Waveform 4 and the threat current of 58 A is well within its capability.

In practice, resistors are often used in series on each data wire for impedance matching, further reducing the incident current and providing an increased guard band for protection of data transfer line interfaces.

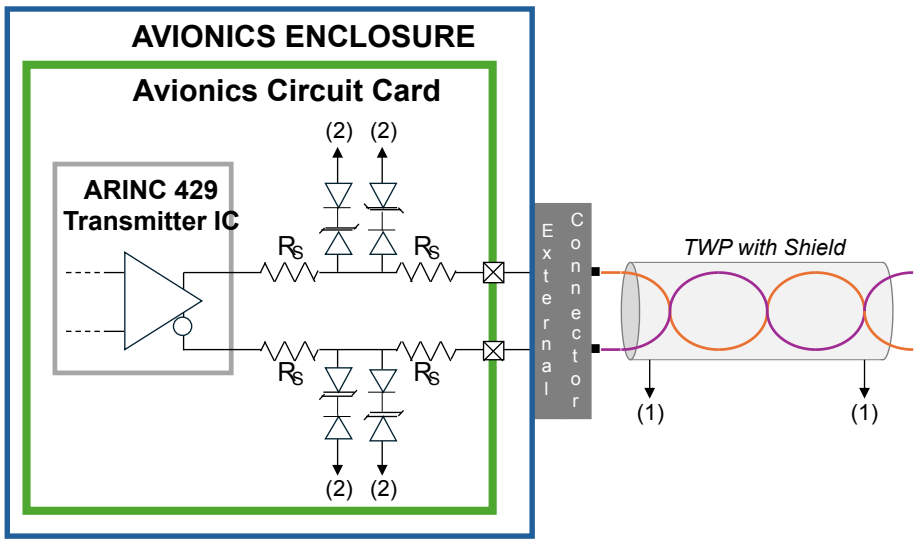
Please be certain that temperature derating is used as applicable. See MicroNote 114 for this and other derating methods that have also been used in the industry. TVS data sheets should show the recommended derating method chosen.

Applications With ARINC 664

Protective devices are always placed from line to common for "common-mode protection" and line to line for differential-mode protection. With many circuits, only common-mode protection on each interface is required since differential mode is provided through termination to circuit ground.

TVS devices must be placed at the point of entry for signals with a direct connection to circuit ground. Shielding is connected to frame ground. For low-capacitance TVS devices, two must be used in antiparallel for bi-directional protection, as shown in Figure 6. See MicroNote 110 for "Parasitic Capacitance in TVS". Using high-speed signals with ARINC 664 requires our "ultra-low" capacitance TVS devices. Those TVS designs are rated with Peak Pulse Power (PPP) @ 10/1000 µs of 150 W (1N8147-1N8182), 500 W (1N8183-1N8218) and 1500 W (1N8219-1N8254) with maximum capacitance values of 4 pF, 10 pF and 15 Pf, respectively. An example will be shown below with the higher PPP rating with the 1N8219 (axial-leaded) or 1N8219US (surface mount) with a low Working Standoff Voltage (VWM) rating of 5.0 V. Higher voltages are also available (up to 170 V) in the 1N8219 through 1N8254 series where VC also increases and IPP decreases changing calculations in equations 10 and 11 below.

Figure 6: Protected High-Speed Line Driver



LEGEND

RS	Series resistors for current limiting and impedance matching. See manufacturer's recommended values.
TVS	Microchip Transient Voltage Suppressor
(1)	Connect to aircraft frame ground
(2)	Connect to avionics internal ground

NOTE: Some transmitter ICs have internal series resistors. If so, that resistance adds to RS in Equations 2, 4 and 8.

An example application with an operating voltage of ±5V can again use equations 8 and 9 for Waveforms 3 and 4 on Threat Level 3 for ARINC 664. Waveform 4 is worst-case with its longer duration. The incident current can also be influenced by added values of R3, as specified by the line driver/receiver manufacturer that will lower the calculated values needed for IPP capabilities by the TVS since it increases the value of Zs in equation 10 below. In this example, we will assume Zs has been increased to 8 ohms with an R3 value of 3 ohms compared to the initial value of 5 ohms in equations 7 and 8. With the same Waveforms and Threat Level shown in equations 8 and 9, the lower value of Peak Impulse Current (IPP) threat for Waveform 4 can then be determined as follows in equation 10:

Equation 10:

IPP = (Voc – Vc) / Zs

= (300V – 11.5V) / 8 ohms, where the Vc is 11.5 V for the 1N8219

= 36 Amps for 6.9/83 ms pulse (Waveform 4) in the RTCA/DO-160G specification

The 1N8219 (VWM = 5 V) with PPP rating of 1500 W has an IPP rating of 130.4 A @ 10/1000 µs. For the shorter Waveform 4 with 6.9/83 µs, the IPP capability can be similarly calculated with a 3.3 multiplication factor from equation 2, as also described in MicroNote 127 in Table 2 for the increase in PP (pulse power) and IP (pulse current).

The IPP can then be calculated as follows:

Equation 11

IPP = 130.4 A × 3.3

= 430 A for a 6.9/83 ms pulse

We observe the 1N8219 is easily capable of withstanding the 36 Amps calculated in equation 10 for Waveform 4 and threat Level 3 with the 430 Amps determined in equation 11. If there is no consideration of an added R3 value of 3 ohms in equation 10, the calculated IPP value would be 58 Amps as previously shown in equation 8 that is still well within the 430 A capabilities of the 1N8219 for faster speeds and “ultra-low” capacitance of 15 pF maximum and the 430 A. Similar calculations for the longer, more severe Waveform 5A threat with 40/120 µs in the RTCA/DO-160G specification and lower source resistance (Zs) of 1 Ohm (instead of 5 ohms in equation 8) will generate a higher IPP of 288.5 A. That is also without adding any value from R3 in Figure 6 that otherwise lowers the calculated threat value. Using a multiplication factor of 2.33 further described in MicroNote 127 Table 2 for Waveform 5A gives an IPP value of 303.8 A for the 1N8219 capability since the 1N8219 has an IPP rating of 130.4 A @ 10/1000 µs. This is still in excess of the 288.5 A needed for a Waveform 5A threat. Higher VWM voltage selections will decline in IPP capability for specific PPP ratings shown in TVS data sheets. This is also shown in MicroNote 132 Graph 14 for 1500 W rated TVS devices including this particular example for the 1500 W rated 1N8219 at 25°C with VWM = 5 V. This lengthy MicroNote 132 (with 22 graphs) also shows performance at elevated temperatures such as 70°C and 100°C for all TVS devices from Microchip (PPP ratings of 150 W to 36,000 W @ 10/1000 µs).

Harsh Environments

In addition to standard products, we also provide options for additional screening where harsh application environments may dictate the need. For flight hardware, we offer avionics-grade component screening, available by adding an MA prefix to the standard part number. This screening is performed on 100% of the production units and includes additional surge tests, temperature cycling and high-temperature reverse bias. For applications where a militarized device is required and no qualified part exists in accordance with MIL-PRF-19500, we offer equivalent JAN, JANTX, JANTXV and JANS designation by adding MQ, MX, MV or MSP prefixes respectively to the standard part number as described in our MicroNote 129 (see review links below).

Summary

The requirements of RTCA/DO-160G have been thoroughly reviewed and this article provides the means of converting surge current ratings at 10/1000 ms on TVS data sheets to voltage and current lightning waveforms specified for aviation in the RTCA/DO-160G specification. This should guide the designer more directly to a given TVS device for a specific requirement.

Derivation of equations for accurately calculating the surge current requirements of any aircraft surge waveform has narrowed the TVS device selection process; however, any added highline long-term voltages (usually tens of milliseconds) should not exceed the minimum breakdown voltage of the TVS.

A similar application note for lightning on aircraft power lines is our MicroNote 127. MicroNote 126 provides guidance in selection through traditional 10/1000 ms waveform conversions. Several examples are provided with equations and conversion tables to aid the design engineer. There is also an extensive “DIRECTselect” method for various waveform threats identified in RTCA/DO-160G in our MicroNote 132 using extensive graphs for our many TVS devices with various PPP ratings from 500 W to 36,000 W @ 10/1000 ms.

We have a wealth of experience in design, manufacturing and applications experience in providing service to the aerospace industry.

Support

For additional technical information, please contact Kent Walters (kent.walters@microchip.com).

Resources

1. MicroNote 110: Parasitic Capacitance in Transient Voltage Suppressors and Low Capacitance Options
2. MicroNote 115: Derating Transient Voltage Suppressors At Elevated Temperatures for Varying Pulse Widths
3. MicroNote 125: Selecting Transient Voltage Suppressors
4. MicroNote 126: Lightning Protection for Aircraft
5. MicroNote 127: Lightning Protection for Aircraft Electrical Power and Data Communication Systems
6. MicroNote 129: Upscreening Commercial TVS Diodes for Aviation and Robust Environments or Applications
7. MicroNote 132: Aircraft Lightning Protection

For more information on this topic, please contact Bill Dillard, Sr. Manager, Business Development, Aerospace and Defense Group at william.dillard@microchip.com

Low-Voltage 32V Battery Management System Demonstration Application

Batteries have become essential to several military systems, from handheld radios to UAVs to future capabilities like lasers, directed energy weapons, hybrid electric tactical vehicles and drones. The move to electrification and dependance on battery systems has made it critical to ensure the battery operates within its safe operating area by monitoring and regulating its state, calculating secondary data, reporting that data, controlling its environment, balancing it if necessary and providing security as well. These functions are performed by the Battery Management System (BMS), thereby improving the safety, life, efficiency and reliability of the battery or battery packs.

The BMS regulates the charging and discharging of the batteries/battery packs and monitors the State of Charge (SOC) and State of Health (SOH) of each individual cell within the pack. The BMS prevents overcharging, over-discharging and overheating. Additionally, the BMS can provide information about the battery pack's performance and health to the user or system controller and even the manufacturer.

In a BMS, monitoring refers to the process of continuously measuring and analyzing various parameters of the battery pack to ensure its safe and efficient operation. These parameters include voltage, current, temperature, SOC, SOH and other relevant data. The BMS uses this information to make decisions about charging, discharging and balancing the battery cells to prevent overcharging, over-discharging, overheating and other potentially dangerous conditions. The monitoring function is critical for maintaining the performance, reliability, efficiency and safety of the battery cells.

There are three main methods of monitoring any given battery's SOC-voltage measurement, Coulomb counting or impedance measurement.

The voltage measurement method measures the voltage across the battery terminal and then correlates it with to SOC value using the discharge curve (voltage vs. SOC) of the battery. This is simple and easy to implement, but due to the battery's internal resistance and its performance drift over time, it may not provide the most accurate reading.

The Coulomb counting method measures the amount of charge that enters or leaves the battery and is a popular choice, especially for online battery type applications that cannot be interrupted for testing. This method is accurate—however, the main drawback of this method is that it requires a current sensor and a complex algorithm to calculate the SOC and it doesn't take into account aging of the batteries and can produce inaccurate results after a few hundred battery cycles.

Impedance measurement estimates the SOC of a battery by measuring the internal resistance of the battery, which changes as the battery discharges and charges. By monitoring the changes in the internal resistance, it is possible to estimate the SOC of the battery. The impedance measurement method is based on the internal resistance increase of the battery as the battery discharges. As the battery charges, the internal resistance decreases, indicating that the active materials are being replenished. This impedance measurement can be used to estimate the SOC of the battery, as well as other battery parameters such as the SOH and State of Function (SOF). The impedance measurement method can be affected by factors such as temperature, age and usage patterns. Therefore, it is often used in combination with other methods, such as voltage and Coulomb counting measurements, to improve the accuracy of the SOC estimation.

In terms of cell balancing, either a passive or active method can be implemented to ensure all cells have the same voltage and SOC, thereby maximizing the performance, efficiency and life of all the cells in a pack.

In a passive cell balancing system, the cells with excess voltage or charge are discharged to the level of the other cells whereas in an active method, the stronger cells are used to charge the weaker cells to equalize their potentials.

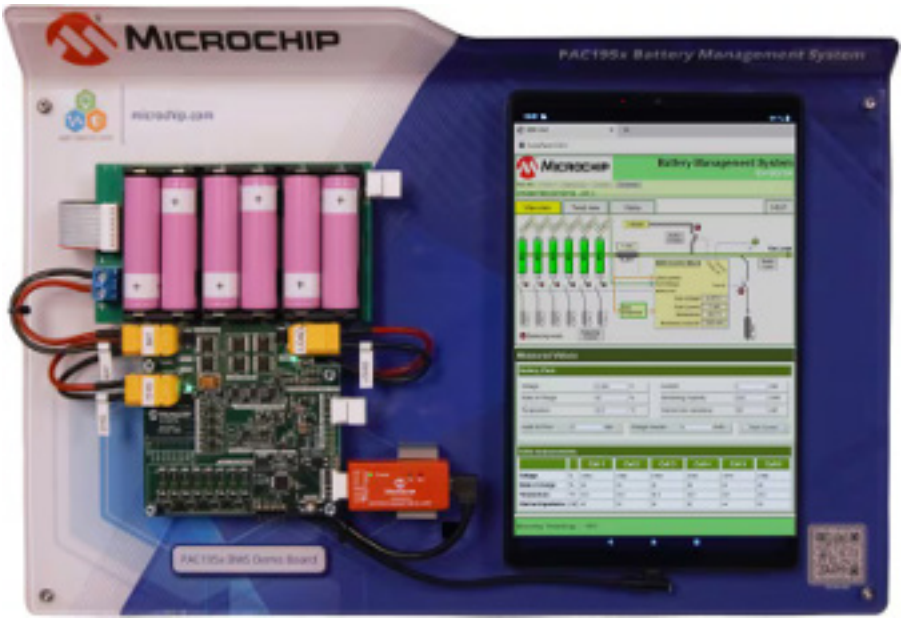
Passive cell balancing utilizes fixed and switching shunt resistors and is a relatively simple and cost-effective solution requiring minimal additional components and does not consume additional power. Passive cell balancing is generally more reliable and has a longer lifespan compared to active cell balancing methods.

Passive cell balancing does have its limitations in that it can only address voltage imbalances, not capacity differences between cells. Additionally, passive cell balancing operates during the charging phase, which means it cannot actively balance cells during discharging or idle period.

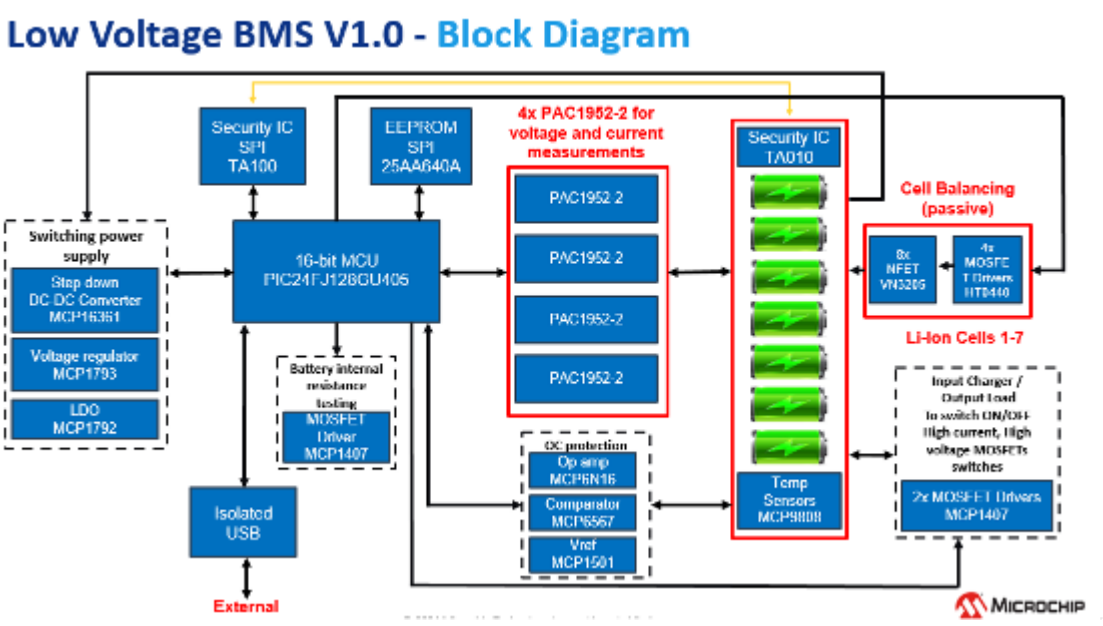
Active cell balancing redistributes charge between cells actively; therefore, cells can be balanced during charging, discharging or idle periods, providing more flexibility and efficiency in maintaining cell balance. The voltage and SOC of each cell is monitored by an electronic control unit and based on this data, it activates the balancing circuitry to transfer charge between cells. Active cell balancing can address both voltage and capacity imbalances, ensuring optimal performance and longevity of the battery pack.

Active cell balancing has the capability to address capacity imbalances, ensuring the energy storage capacity is optimized. Active cell balancing can compensate for aging or manufacturing variations by adapting to changing cell characteristics.

Our low-voltage BMS reference design demonstrates monitoring a stack of 6 to 8 series 18650 Li-Ion batteries using the PAC1952 analog front-end. This battery management solution offers state-of-charge determination using all three methods demonstrated in this post: voltage measurement, Coulomb counting and impedance measurement to enable accurate monitoring of battery cells. In addition, this demo supports passive cell balancing using a network of discrete FETs and resistors. It also comes with GUI support showing battery cells' SOC in real time.



Low Voltage BMS V1.0 Block Diagram



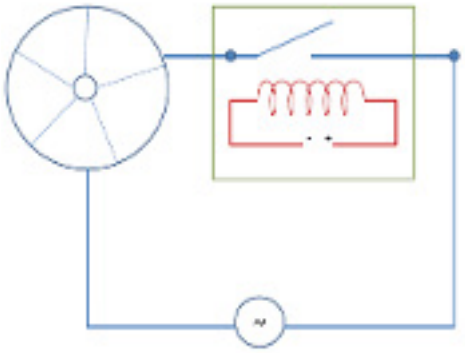
For any questions or comments regarding this newsletter, please feel free to contact Emil Verano, District Client Engagement Manager, at emil.verano@microchip.com.

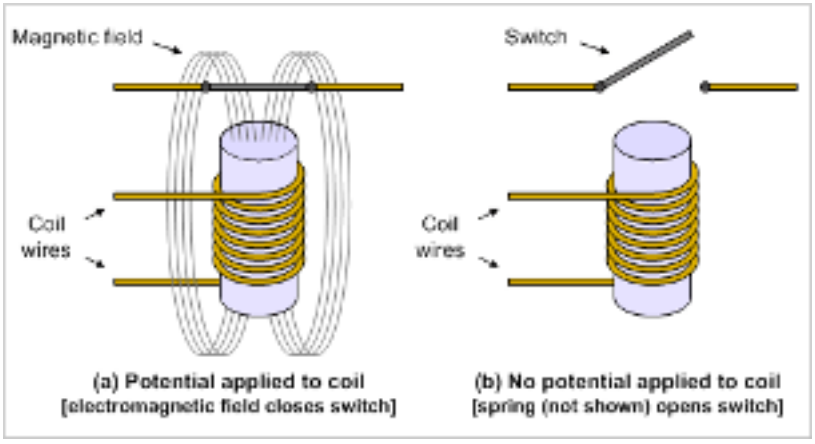
Amit's Tech Corner

By Amit Gole, Product Marketing Manager, Discrete Products Group; amit.gole@microchip.com

Electromechanical Power Relays for Mission-Critical and High-Reliability Applications

Relay definition: A relay is an electrically operated switch that is remotely activated by an electromagnet, which pulls a set of contacts to either make or break a circuit.





Key Functions of Relays:

- Galvanic separation of circuits (example: separation of AC and DC circuits)
- Capability to have single input/multiple output
- Multiple switching operations (time delay, signal and more)
- Interface between electronic and power circuits

How Do Relays Work?

Relays convert an electrical input signal on the primary side of the circuit to an intermediate and non-electric physical signal. These devices also reconvert the non-electric physical signal to operate a switching element (secondary side), such as contacts, which switch and conduct electrical current (i.e., output, load current). Relays use the non-electric signal between the primary and secondary side to provide the necessary galvanic separation between the input and output circuits. Relays enable a single output that can activate multiple circuits and functions.

Non-Latching Relays and Latching Relays

Relays come with several sets of contacts to change over multiple contacts (circuits). The contacts could wither normally open or normally closed. This depends on whether a relay is activating or opening a circuit. Normally Open (NO) contact state is the state when contact is open with relay at rest. Normally Closed (NC) contact state is the state when contact is closed with relay at rest. NO relays are more commonplace than NC relays.

Non-latching relays stay in continuous NC position without power supply. As the power flows through the relay-coil, the relay switches to a NO position and remains as long as the power is applied. Once power is switched off, the non-latching relay returns to its static NC position. Latching relays are also called "bistable" relays.

Non-latching and latching relays are similar in design and function, except that the latching relay will remain in the position it was last powered while a non-latching relay that returns to its normal position power is removed from the coil. The "latching" characteristic offers benefits in conversation of energy and is chosen based on the need of the applications. Latching relays retain the switched position after interruption of the energizing current through the coil by a permanent magnet. Latching relays turned to reset by counter-energizing the coil.

What Are Electromechanical Power Relays?

Electromechanical power relays are switches that control high-power electrical circuits using a low-power signal. They consist of an electromagnet, an armature, a spring and a series of electrical contacts. When an electrical current flows through the coil of the electromagnet, it creates a magnetic field that attracts the armature, causing it to move and either make or break a connection with the contacts. This operation allows the relay to control an electrical circuit without the need for direct mechanical action from the user.

Power relays are designed to handle larger amounts of current and voltage than smaller signal relays. They are commonly used in applications where it is necessary to control high-power or high-voltage equipment with a low-power control signal, such as in industrial machinery, automotive systems and large-scale electrical systems. The use of relays ensures that control circuits can operate safely and with lower energy requirements, isolating the control circuit from the high-power circuit.

Electromechanical versus Solid State Relay (SSR) Characteristics Comparison

Highlighted are some of the tenets of electromechanical power relays that make their use more common for high-reliability and harsh-environment applications compared to Solid State Relays (SSRs). It is because of these tenets that electromechanical relays are used prominently in most demanding applications such as aviation, military, space, downhole drilling (oil and gas), transportation and railways.

Characteristics	Electromechanical Relays	Solid State Relays (SSRs)
Sensitivity to withstand misuse or misapplication	Good	Poor
Sensitive to corrosion, oxidation or contaminates	Yes	No
Sensitive to shock, vibration or acceleration	Yes	No
Sensitivity to radiation	Fair	Poor
Package versatility	Good	Fair
Cost per pole	Best	Fair
Compatibility of military/aerospace specifications	Good	Poor
Ease of troubleshooting	Good	Poor
Derating of output current required above TA=25°C	No	Yes
Heatsink required to switch maximum rated loads	No	Yes
Sensitivity (susceptibility) to EMI/RFI false operation	No	Yes
Sensitive to Electrostatic Discharge (ESD) turn-on	No	Yes
Sensitive to overvoltage turn-on	No	Yes
Sensitive to thermal turn-on	No	Yes
Sensitive to dv/dt turn-on	No	Yes
Sensitive to load di/dt turn-on	No	Yes
Capable of dry circuit load switching	Yes	No
Capable of coaxial load (RF) switching	Yes	No

Key Determinants of Relay Reliability:

Application dependent:

- Selection of relay for application
- Electrical parameters of load within specifications
- Coil operating parameters
- Ambient temperature
- Mechanical stress
- Climate and humidity
- Processing during assembly

Manufacturing dependent:

- Selection of proper material
- Appropriate design
- Optimal production process
- Storage conditions
- Choice of transport

Our High-Reliability Electromechanical Power Relays and Adjacent Offerings

For over 60 years, we've established a formidable reputation for delivering high-quality, mission-critical electromechanical power relays for aerospace applications. Our space-grade relays have a proven flight history in groundbreaking projects such as Mars rovers and the International Space Station. These relays adhere to strict MIL-STD-approved materials and maintain an ISO 5-compliant environment during manufacturing. The extensive testing laboratory and manufacturing expertise enables us to offer custom solutions that meet the rigorous NASA-EEE-INST-002 standards and provide exceptional protection against harsh environments, pollutants and contaminants.

Advantages of Our Relays

- Spectrum of current ratings that offers flexibility
- Adherence to MIL-PRF-83536, 61016, 39016 and 5757 standards
- High reliability that withstands the harsh conditions of the most demanding space and defense applications
- Rated current of 100,000 cycles and 400,000 cycles of mechanical life
- Military qualification (QPL) and custom parts availability

Key Applications:

- Space: Propulsion for rockets (rocket motors), rovers on planets (Mars Rover)
- Aviation: Commercial aviation, helicopters, military fighters
- Defense: Missiles, amphibian attach vehicles, launchers, armored vehicles
- Transportation: Railway power distribution panels, mining vehicles, automotive
- Downhole drilling: Offshore/onshore oil and gas rigs


Space


Aviation


Defense


Transportation


Downhole Drilling

Our product portfolio contains products that serve the applications above such as space-grade relays, QPL relays and custom relays.

Space-grade relays: These relays meet stringent specifications, such as NASA-EEE-INST-002 and the common MIL-R-83536 specification. They are available in magnetic latching, suppressed and non-suppressed types in hermetically sealed packaging to protect against harsh environments.

Figure 1: Our Exemplary Flight Heritage

NASA-INST-002 Space Specifications			
Test	**Level I**	**Level II**	**Level III**
Cleaning and small particle inspection	30× microscope class 100 clean room filter particles > 0.001"	30× microscope class 100 clean room filter particles > 0.001"	NA
Visual and mechanical inspection (internal)	Verify materials and workmanship	Verify materials and workmanship	Verify materials and workmanship
Visual and mechanical inspection (external)	Materials, interface, construction, dimensions, marking	Materials, interface, construction, dimensions, marking	NA
Dielectric withstanding voltage	100 µA or 1 Ma with test voltage	NA	NA
Insulation resistance	100 or 10K megohms > @500 volts ±10%	NA	NA
Electrical characteristics	Per device specification	NA	NA
Vibration (sinusoidal)	20 or 30 Gs	NA	NA
PIND	27 Hz @ 5G	27Hz @ 5G	27Hz @ 5G
Screening, internal moisture	IR >10,000 MΩ @ 2.5 min Coil Energizad	IR >10,000 MΩ @2.5 min Coil Energizad	NA
High-temperature soak 16 hours @ max-rated operating temperature	16 HR@ 120% Load	NA	NA
Run-in screening	2,500 Cycles @ 125 ºC and −65 ºC	2,500 Cycles @ room @ 125 ºC and −65 ºC	NA
Radiographic inspection	MSFC-STD-355C	NA	NA
Seal	1 × 10-6 Atm cm 3/Sec air.	1 × 10-6 Atm cm 3/Sec air.	NA
Electrical characteristics	Per spec call out	Per spec call out	Per spec call out
Percent Defective Allowable (PDA)	5%	15%	NA
Solderability	350 ºC for 5 Seconds	350 ºC for 5 Seconds	350 ºC for 5 Seconds

Figure: NASA-INST-002 Space Specifications

QPL-grade relays: As the name suggests, these are designated Qualified Products List (QPL) relays as per the U.S. government. The U.S. government's Qualified Products List (QPL) is a list of products that has been rigorously reviewed and tested to ensure it meets a specific set of quality and performance requirements as defined by the Defense Supply Center. To get on the list, products must pass a series of stress and performance tests every five years. Microchip has decades of heritage and our relays are qualified to M83536 and M6106 specifications.

MIL-PRF-83536, MIL-PRF-39016 Specifications		
Test	**MIL-PRF-83536**	**MIL-PRF-39016**
Cleaning and small particle inspection	NA	NA
Visual and mechanical inspection (internal)	Verify materials and workmanship	Verify materials and workmanship
Visual and mechanical inspection (external)	Materials, interface, construction, dimensions, marking	Materials, interface, construction, dimensions, marking
Dielectric withstanding voltage	1 mA with test voltage (AC or DC)	100 µA with test voltage (AC or DC)
Insulation resistance	100 megohms or > @500 volts ±10%	100 megohms or > @500 volts ±10%
Electrical characteristics	Per device specification	Per device specification
Vibration (sinusoidal)	.0.12" DA 10 - 70 Hz 30 Gs 70 - 3,000 Hz	0.4" DA 10 - 38 Hz, 20 Gs 38 - 2,000 Hz
PIND	NA	NA
Screening, internal moisture	IR >100 MΩ @ 2.5 min Coil Energizad	IR >10,000 MΩ @2.5 min Coil Energizad
High-temperature soak 16 hours @ maximum-rated operating temperature	NA	NA
Run-in screening	2,500 Cycles @ 125 ºC and −65 ºC	2,500 Cycles @ 125 ºC and −65 ºC
Radiographic inspection	NA	NA
Seal	1 x 10-6 Atm cm 3/Sec air	1 x 10-6 Atm cm 3/Sec air
Electrical characteristics	Per spec call out	Per spec call out
Percent Defective Allowable (PDA)	NA	NA
Solderability	350 ºC for 5 Seconds	350 ºC for 5 Seconds

Figure: MIL-PRF-83536, MIL-PRF-39016 Specifications

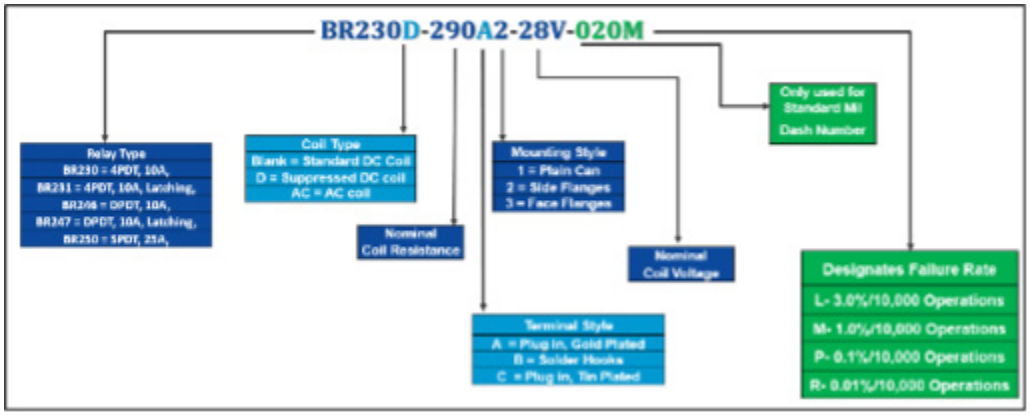


Figure: Part Numbers for QPL Relays

Series		BR230	BR230D	BR231	BR231D	BR246	BR246D	BR247
Features		Miniature Low level to 10A All-welded construction	Miniature 10A All-welded construction DC-suppressed coils	Miniature Low level to 10A All-welded construction Magnetic latching	Miniature 10A All-welded construction Magnetic latching DC-suppressed coils	Miniature Low level to 10A All-welded construction	Miniature 10A All-welded construction DC-suppressed coils	Miniature Low level to 10A All-welded construction Magnetic latching
Hermetically Sealed		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Contacts	Form	4 Form C	4 Form C	4 Form C	4 Form C	2 Form C	2 Form C	2 Form C
	Rating (Resistive)	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}	10-50 µA @ 10-50 mV 10A @ 28 V_{DC} or 115 V_{AC}
Coil Voltage		6, 12, 28, 48 V_{DC}, 115 V_{AC}	6, 12, 28, 48 V_{DC}	6, 12, 28, 48 V_{DC}, 115 V_{AC}	6, 12, 28, 48 V_{DC}	6, 12, 28, 48 V_{DC}, 115 V_{AC}	6, 12, 28, 48 V_{DC}	6, 12, 28, 48 V_{DC}, 115 V_{AC}
Operating Power at Pick-Up Voltage		500 mW	500 mW	500 mW	500 mW	500 mW	500 mW	500 mW
Dielectric Strength		Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms
Typical Life Operations (at Rated Load)	Electrical	100,000	100,000	100,000	100,000	100,000	100,000	100,000
Maximum Size in Inches (L × W × H) (Less Mounting Brackets)		1.025 × 1.025 × 1.010	1.025 × 1.025 × 1.010	1.025 × 1.025 × 1.010	1.025 × 1.025 × 1.010	1.025 × 0.525 × 1.010 or 1.125	1.025 × 0.525 × 1.010 or 1.125	1.025 × 0.525 × 1.010 or 1.125
Terminals	Plug-In	X	X	X	X	X	X	X
	Solder Pin	X	X	X	X	X	X	X
	Solder Hook	X	X	X	X	X	X	X
MIL-SPEC Type (Reference)		Qualified to MIL-PRF-83536	Qualified to MIL-PRF-83536	Qualified to MIL-PRF-83536	Qualified to MIL-PRF-83536	Qualified to MIL-PRF-83536	Qualified to MIL-PRF-83536	Qualified to MIL-PRF-83536

Figure: Catalog Offerings of Space-Grade and QPL Relays

Series		BR247D	BR250	BR250D	700	701	702	703
Features		Miniature 10A All-welded construction Magnetic latching DC-suppressed coils	Miniature 25A All-welded construction	Miniature 25A All-welded construction DC-suppressed coils	Remote power controller Up to 200A Auxiliary contacts available AC-only applications	Remote power controller Up to 200A Auxiliary contacts available DC-only applications	Remote power controller Up to 200A Auxiliary contacts available AC/DC applications	Remote power controller Up to 100A Auxiliary contacts available AC 3-Phase applications
Hermetically Sealed		Yes	Yes	Yes	No	No	No	No
Contacts	Form	2 Form C	1 Form C	1 Form C	1 Form X	1 Form X	1 Form X	3 Form X
	Rating (Resistive)	10A @ 28 V_{DC} or 115 V_{AC}	25A @ 28 V_{DC} or 115 V_{AC}	25A @ 28 V_{DC} or 115 V_{AC}	Up to 200A @ 115 V_{AC}	Up to 200A @ 28 V_{DC}	Up to 100A @ 115 V_{AC} or 28 V_{DC}	Up to 200A @ 115 V_{AC} or 208 V_{AC}
Coil Voltage		6, 12, 28, 48 V_{DC}	6, 12, 28, 48 V_{DC}, 115 V_{AC}	6, 12, 28, 48 V_{DC}	28 V_{DC}	28 V_{DC}	28 V_{DC}, 115 VAC	28 V_{DC}
Operating Power at Pick-Up Voltage		500 mW	500 mW	500 mW	N/A	N/A	N/A	N/A
Dielectric Strength		Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1500 Vrms Between open contacts: 1350 Vrms	Between all points: 1500 Vrms Between open contacts: 1350 Vrms	Between all points: 1500 Vrms Between open contacts: 1350 Vrms	Between all points: 1500 Vrms Between open contacts: 1350 Vrms
Typical Life Operations (at Rated Load)	Electrical	100,000	100,000	50,000	50,000	50,000	50,000	50,000
Maximum Size in Inches (L × W × H) (Less Mounting Brackets)		1.025 × 0.525 × 1.010 or 1.125	1.025 × 0.525 × 1.010 or 1.125	1.025 × 0.525 × 1.010 or 1.125	4.260 × 1.200 × 3.250	4.260 × 1.200 × 3.250	4.260 × 1.200 × 3.250	4.260 × 3.690 × 2.250
Terminals	Plug-In	X	X	X	MIL-C-39029 Connector	MIL-C-39029 Connector	MIL-C-39029 Connector	MIL-C-39029 Connector
	Solder Pin	X	X	X				
	Solder Hook	X	X	X				
MIL-SPEC Type (Reference)		Qualified to MIL-PRF-83536	Qualified to MIL-PRF-6106	Qualified to MIL-PRF-6106	Designed to meet MIL-PRF-83383	Designed to meet MIL-PRF-83383	Designed to meet MIL-PRF-83383	Designed to meet MIL-PRF-83383

Custom relays: Custom relays encompass relays that are made to specification according to customer needs to meet highly specific design requirements and stringent MIL-compliance, such as for mission-critical designs, harsh environments or a combination of all these factors. We are one of the few suppliers that can support highly customized designs for relays and Remote Power Controllers (RPCs).

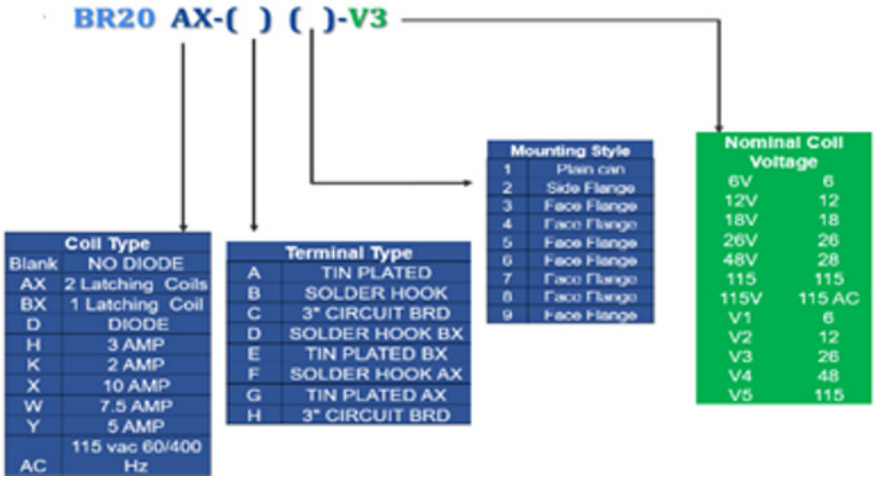


Figure: Part Numbers for Custom Relays

Series		BR8	BR13	BR15	BR19	BR20	BR23	BR24
Features		Crystal can Dry circuit to 2A All-welded construction	Crystal can Dry circuit to 5A All-welded construction	Crystal can Dry circuit to 10A All-welded construction	Crystal can Dry circuit to 10A All-welded construction	Crystal can Dry circuit to 10A All-welded construction Magnetic latching	Crystal can Dry circuit to 10A All-welded construction Magnetic latching	Crystal can Dry circuit to 10A All-welded construction Suppressed coil available
Hermetically Sealed		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Contacts	Form	2 Form C	2 Form C	4 Form C	2 Form C	2 Form C	4 Form C	2 Form C
	Rating (Resistive)	10–50 µA @ 10–50 mV 2A @ 28 V_{DC} or 115 V_{AC}	5A @ 28 V_{DC} or 115 V_{AC} 3A @ 28 V_{DC} or 115 V_{AC} 2A @ 28 V_{DC} or 115 V_{AC}	10 mA @ 30 mV 10A @ 28 V_{DC} or 115 V_{AC} 7.5A @ 28 V_{DC} or 115 V_{AC} 5A @ 28 V_{DC} or 115 V_{AC}	10 mA @ 30 mV 10A @ 28 V_{DC} or 115 V_{AC} 5A @ 28 V_{DC} or 115 V_{AC}	10 mA @ 30 mV 10A @ 28 V_{DC} or 115 V_{AC}	10 mA @ 30 mV 10A @ 28 V_{DC} or 115 V_{AC}	10–50 µA @ 10–50 mV 10A @ 28 V_{DC} or 115 V_{AC}
Coil Voltage		6, 12, 26, 115 V_{DC}	6, 12, 26, 115 V_{DC}	6, 12, 26, 115 V_{DC}, 115 V_{AC}	6, 12, 26, 48, 115 V_{DC}, 115 V_{AC}	6, 12, 26, 48, 115 V_{DC}	6, 12, 26, 48, 115 V_{DC}	6, 12, 26 V_{DC}
Operating Power at Pick-Up Voltage		250 mW or 150 mW	250 mW, 150 mW or 40 mW	1000 mW, 500 mW or 400 mW	500 mW or 175 mW	250 mW or 130 mW	500 mW or 250 mW	400 mW
Dielectric Strength		Between all points: 1000 Vrms Between open contacts: 750 Vrms	Between all points: 1000 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms	Between all points: 1250 Vrms Between open contacts: 1250 Vrms
Typical Life Operations (at Rated Load)	Electrical	100,000	100,000	100,000	100,000	100,000	100,000	100,000
Maximum Size in Inches (L × W × H) (Less Mounting Brackets)		0.790 × 0.360 × 0.870 or 1.190	0.810 × 0.410 × 0.900 or 1.29	1.075 × 1.000 × 1.300	1.075 × 0.515 × 1.300	1.075 × 0.515 × 1.300	1.075 × 1.000 × 1.300	1.015 × 0.515 × 0.885
Terminals	Plug-In	-	-	-	-	-	-	-
	Solder Pin	X	X	X	X	X	X	X
	Solder Hook	X	X	X	X	X	X	X
MIL-SPEC Type (Reference)		MIL-R-5757	MIL-PRF-39016	MIL-PRF-39016	MIL-PRF-39016	MIL-PRF-39016	MIL-PRF-39016	MIL-PRF-39016

Figure: Custom and Legacy Relays

Manufacturing process: Power relays have highly nuanced manufacturing and assembly processes that requires strong design, engineering and operational capabilities to achieve the desired quality for high-reliability applications. It takes more than 100 parts to make an electromechanical relay and more than 120 parts to build a BR230 4PDT 10-amp QPL relay.

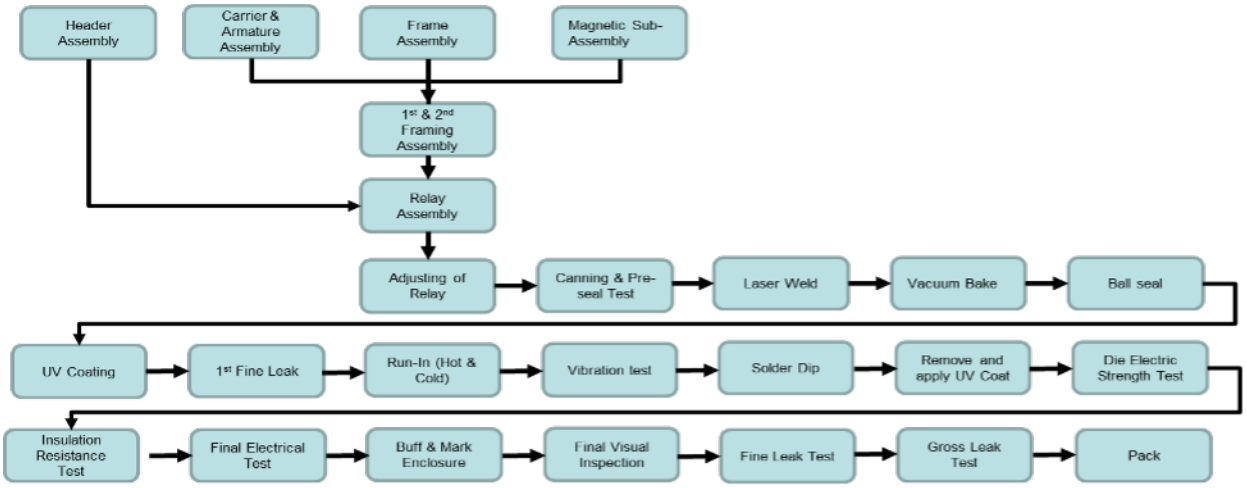


Figure: Standard Process Flow for Electromechanical Relays

Figure: Typical Relay Assembly Process

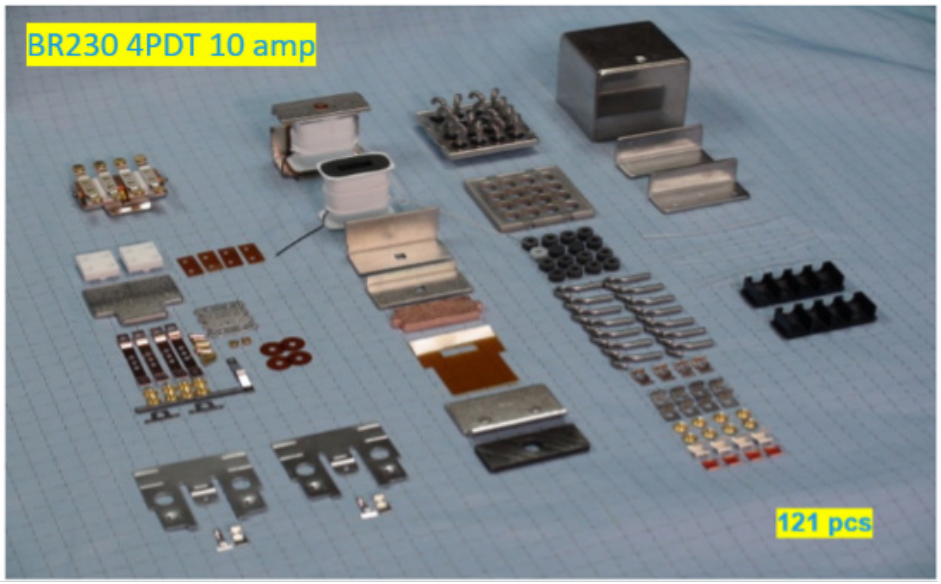


Figure: Complexity of Relay Assembly

Manufacturing Capabilities:

- Quality system MIL-STD-790 & ISO-9001 certified
- Single lot with full traceability
- MIL-Pore cleaning
- PreCap with source inspection option
- E-beam, spot and Laser welding
- Metal brazing, etching, heat treat, micro-sectioning
- Electro-chemical metal marking
- Conformal coating
- Bonding, adhesives, masking
- Gas mixture back-filling
- Hermetic sealing inert and controlled atmosphere
- Solder dip
- Ionic cleaning and fluorocarbon cleaning
- Stamping, machining and tool making
- Metal working, polishing and tumbling
- ISO 5 (class 100) cleanroom assembly
- Vacuum bake sealing to 10 -10 atm.cc/s

Testing Capabilities:

- ATP and all Grp-A screening data record, serialization
- Lot acceptance LAT performed and data-recorded testing
- Survivability shock to 2000Gs
- Survivability vibe to 50Gs sine and random
- Motor, inductive, capacitive, rupture and time current load testing
- Load testing 28VDC–1400 ADC, 400 Hz three-phase, A/C up to 350 Amps
- Current transient up to 1200 ADC
- Particle capture
- Cold/hot miss test
- Ultra-high vacuum testing
- Humidity and moisture
- Fine leak to 10 -10, gross leak
- Thermal shock
- Life test
- DPA
- XRF
- RGA
- PIND
- X-RAY

General Specifications: These are the generic specifications. Please refer to our brochure for more details.

Coil Input Voltage	6 Vdc, 12 Vdc, 18 Vdc, 26 Vdc, 48 Vdc, 115 Vdc, 115/208 VAC @ 400Hz or 50/400Hz
Coil Power Watts	0.040 W to 1.00 W
Number of poles	1 PST, 1 PDT, 2 PDT, 4 PDT
Load Voltage	0.010–.0050, 28 VDC, 115 VAC
Load Current Amps	0.010–0.050 Amps, 2 , 3, 5, 7.5, 10, 15 and 25
Resistive Load Rating	100%
Inductive Load Rating	80%
Motor Load Rating	40%
Lamp Load Rating	20%
Life Cycles at Rated Load	Rated for 100,000 operations at rated resistive load and 400,000 operations at 25% rated load.
Temperature Limits	−70 ºC to 125 ºC; high temp version (−40 ºC to +200ºC)
Insulation Resistance @500Vdc	Up to 10 GΩ
Dielectric	500 VAC to 2500 VAC/DC
Contact Resistance in Ohms	0.006 Ω to 0.050 Ω
Shock	50 Gs 11 ms, 200 Gs 6 ms
Vibration	0.4" DA 10–38 Hz, 20 Gs 38–2,000 Hz and 0.12 DA 10–70 Hz, 30 Gs 70–3,000 Hz
Qualification	MIL-PRF-83536, MIL-PRF-39016, EEE-INST-002
Mounting	As customer design requires
Pin Configuration	Solder hook, straight plug-in
Contact Bounce	2 ms max @ 2 Amps
Contact Resistance	20 mΩ @ 2 Amps
Operate/Release Time	4 ms to 15 ms Max
Duty Cycle	Continuous
Radiation	TID and SEE immune

Salient Features:

- All welded construction
- Hermetically sealed to 1 X10-6 atm.cc/s
- Suppressed or non-suppressed
- Inductive spike suppression bifilar wounded coils
- Arc shields to ground case
- Continuous duty cycle
- 100% Group A testing
- Data pack, recorded data, serialization and Lot ID marking
- Patented 30-Amp vacuum relay stand-off up to 8 KV
- High temperature relays up to 200°C

References:

- https://www.te.com/en/products/relays-and-contactors/relays.html
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- https://www.microchip.com/en-us/products/power-management/power-relays
- https://na.industrial.panasonic.com/blog/difference-between-latching-and-non-latching-relays

For more information on this topic, please contact Amit Gole, our Product Marketing Manager in the Discrete Products Group, at amit.gole@microchip.com.

Future Topics Planned for This Newsletter

A note to our readers: if you have a specific topic of interest, please email eli.kawam@microchip.com and we will do our best to address this topic.

- Missiles and guided munitions
- Electrification, ground vehicles and more electric systems over hydraulic and pneumatic systems
- Actuation reference design
- RTEMS on PolarFire SoC
- Mi-V ecosystem for PolarFire SoC
- JOTP-51 compliance using PolarFire FPGAs
- PMIC
- Review an additional MicroNote