PIC64-HPSC Series

PIC64-HPSC1000 and PIC64-HPSC1100

Summary

The PIC64-HPSC (High-Performance Spaceflight Computing) series of 64-bit microprocessors (MPUs) represents a revolutionary step forward in radiation-hardened and radiation-tolerant processors. Offering a 100× improvement in processing capability compared to traditional space processors and bringing new capabilities to space such as virtualization, AI, TSN Ethernet, RDMA over Converged Ethernet v2, PCIe®, Compute Express Link® (CXL®) 2.0 and post-quantum cryptography, PIC64-HPSC redefines what is possible for the future of space exploration and space processing. The PIC64-HPSC1000 and PIC64-HPSC1100 family includes multiple device versions in the same hardware and software footprint to meet mission profiles ranging from Low Earth Orbit (LEO) to Deep Space.

A complete package of tools, libraries, drivers and boot firmware is available to unlock the full capabilities of HPSC while accelerating your time to market. Multiple open source, commercial and real-time operating systems are supported including Linux® and RTEMS, as well as hypervisors such as Xen. HPSC leverages and builds upon Microchip's Mi-V ecosystem for RISC-V®.

Application Compute Complex With Real-Time Support

The PIC64-HPSC1000 and PIC64-HPSC1100 family provides multicore 64-bit RISC-V processing. Highlights of the Application Compute Complex include:

- Eight 64-bit RISC-V CPU cores (SiFive Intelligence™ X280) with vector extensions
- Up to 1 GHz operation
- Optional Dual-Core Lockstep (DCLS)
- Multiple operating modes: Unified, Split and Cache-Isolated
- Enhanced support for real-time applications
- Decoupled vector pipeline supporting 512-bit vector lengths that enable AI/ML
- Support for virtualization and both Type 1 and Type 2 hypervisor usage (MMU and IOMMU with two-stage translation)
- 26K DMIPS (CoreMark® score of 46K) for scalar performance and up to 2 TOPS (int8) or 1 TFLOPS (bfloat16) for vector matrix multiplication (all eight cores)

WorldGuard End-to-End Partitioning Architecture

WorldGuard provides hardware-based spatial partitioning of the entire device including core, cache, interconnect, peripherals and memory with support for up to 32 domains. WorldGuard facilitates integration and isolation of mixed-criticality workloads.

Integrated System Controller

The onboard System Controller is an additional 64-bit RISC-V CPU core (SiFive S7) operating at 500 MHz. The system controller enables mission-critical and autonomous systems with runtime monitoring and fault management. Attached to the system controller are the following dedicated and shared peripherals:

- Two SPI/QSPI
- 2x NOR Flash/SRAM (shared)
- One I^2C, one UART and 32 GPIO (shared)
- One SpaceWire (emergency mode only)

TSN Ethernet Switch

PIC64-HPSC1000 and PIC64-HPSC1100 family integrates 240 Gbps of Ethernet switching with full TSN support aligned to P802.1DP (aerospace profile):

- Up to 160 Gbps of switching from up to 16 external facing ports
- Up to 80 Gbps of Direct Memory Access (DMA) for packet insertion and extraction from internal subsystems, including the Application Compute Complex
- 16 external-facing ports for Ethernet rates from 10M to 10G
- Remote Direct Memory Access (RDMA) with RDMA over Converged Ethernet (RoCEv2) for low-latency transfers from remote sensors and extensibility

Memory Interfaces

- Two DDR interfaces supporting DDR3-2133 or DDR4-3200
- 72-bit interface with ECC for single-bit error correction
- Optional 80-bit interface composed of x8 memory devices for multi-bit error correction and memory chip failure protection
- Up to 32 GB per DDR interface

Nonvolatile Memory and SRAM

- Parallel NAND Flash, NOR Flash and SRAM
- NAND and NOR SPI Flash
- MRAM with SPI or parallel interface

Co-Processor/Accelerator Interfaces

- Up to two PCIe Gen 3 ×8 ports or four PCIe Gen 3 ×4 ports through bifurcation
- Support for CXL 2.0 (at 8 GT/s) host operation for cache-coherent interconnect to CXL Type 2 devices such as FPGAs, GPUs or coprocessors

SpaceWire Interfaces

- Seven RMAP-compatible SpaceWire ports with internal routers
- One SpaceWire port for emergency access
- Support for rates from 10 Mbps to 200 Mbps

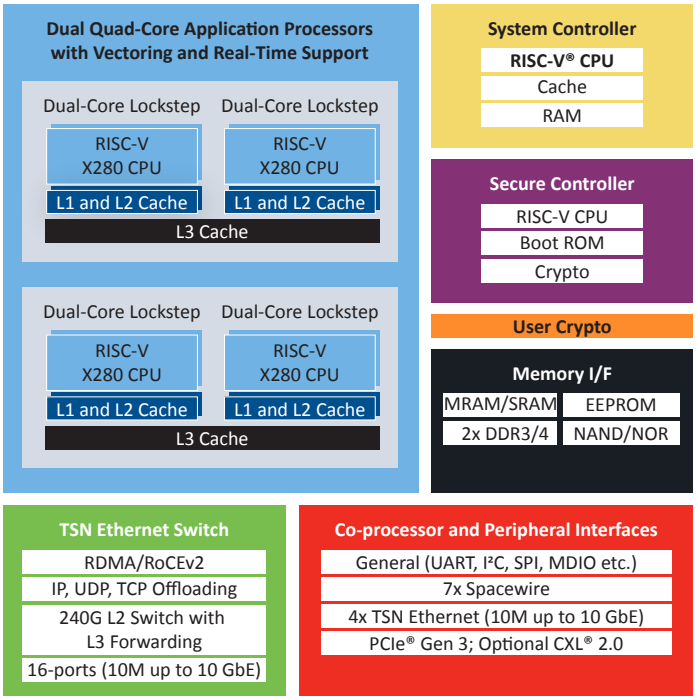
Peripheral Interfaces

- Up to four TSN Ethernet endpoint ports supporting rates from 10M to 10G
- Two SPI, four UART, four I^2C, 64 GPIO, two MDIO, JTAG host, timers and watchdogs

Defense-in-Depth Security

- Cryptographically controlled supply chain and device manufacturing flow that ensures authenticity
- Dedicated secure enclave to support secure boot and platform root of trust
- Full support for post-quantum cryptography: ML-KEM and ML-DSA
- User/application-level security acceleration
- Extensive anti-tamper detection and response capabilities

PIC64-HPSC Block Diagram



Product Table

	PIC64-HPSC1000-RH	PIC64-HPSC1100-RT	PIC64-HPSC1000-EM/ PIC64-HPSC1100-EM
Product Class	Radiation Hardened	Radiation Tolerant	Engineering Model
Application	MEO, GEO, Deep Space	LEO	Lab Development
Qualification Level	QML-Y	JEDEC JESD47	JEDEC JESD47
TID	100 krad (test to 200 krad)	50 krad	Not Applicable
SEL	78 MeV	42 MeV	Not Applicable
Operating Temperature	−55°C (Ta) to +125°C (Tj)	−55°C (Ta) to +125°C (Tj)	0°C (Ta) to +70°C (Tj)

Contact Microchip for the fully qualified part number.