Radiation-Tolerant FPGAs

MICROCHIP

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Space Solutions

Taking Designs From Earth to Outer Space

Our high-reliability, low-power spaceflight FPGAs are your best design choice for low Earth orbit, deep space or anything in between. With a history of providing the most reliable, robust, low-power SONOS, Flash- and antifuse-based FPGAs in the industry, we offer the best combination of features, performance and radiation tolerance.

In addition to FPGAs, we provide radiation-hardened and radiation-tolerant solutions ranging from diodes, transistors and power converters to ASICs, RF components, oscillators and timing products to mixed-signal integrated circuits, custom semiconductor packaging and integrated power distribution systems.

Radiation-Tolerant FPGAs

Delivering High-Speed Signal Processing and High Reliability Command and Control

Our FPGAs facilitate the design of high-speed communications payloads, high-resolution sensors and instruments and flight-critical systems that enable tomorrow's space missions. Only we can meet the power, size, cost and reliability targets that reduce time to launch and minimize cost and schedule risks.

Flight Heritage

RTSX-SU FPGAs

- Flight heritage since 2005
- EAR-controlled
- QML class Q qualified

RTAX™ FPGAs

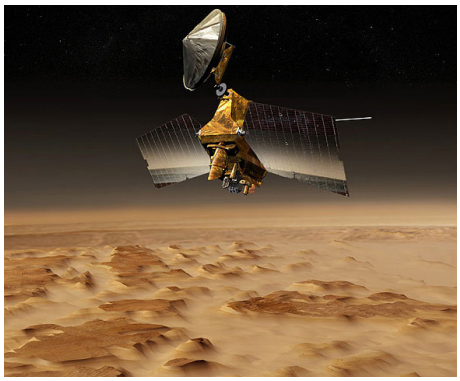
- Flight heritage since 2007
- On-board SRAM and DSP Mathblocks
- EAR-controlled
- QML class V qualified

RT ProASIC® 3 FPGAs

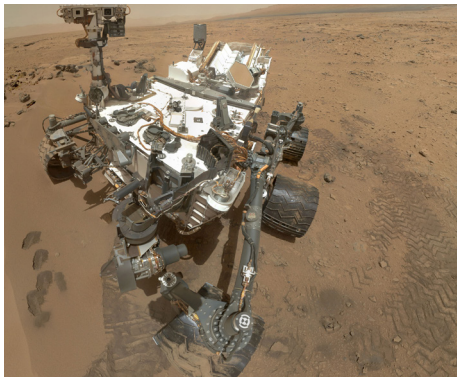
- Flight heritage since 2013
- First Flash-based RT FPGA in space
- EAR-controlled
- QML class Q qualified

RTG4™ FPGAs Flight Heritage

- Flight Heritage since 2019
- First Flash Based Rad Hard by Design FPGA in space
- EAR-Controlled
- QML Class V Qualified



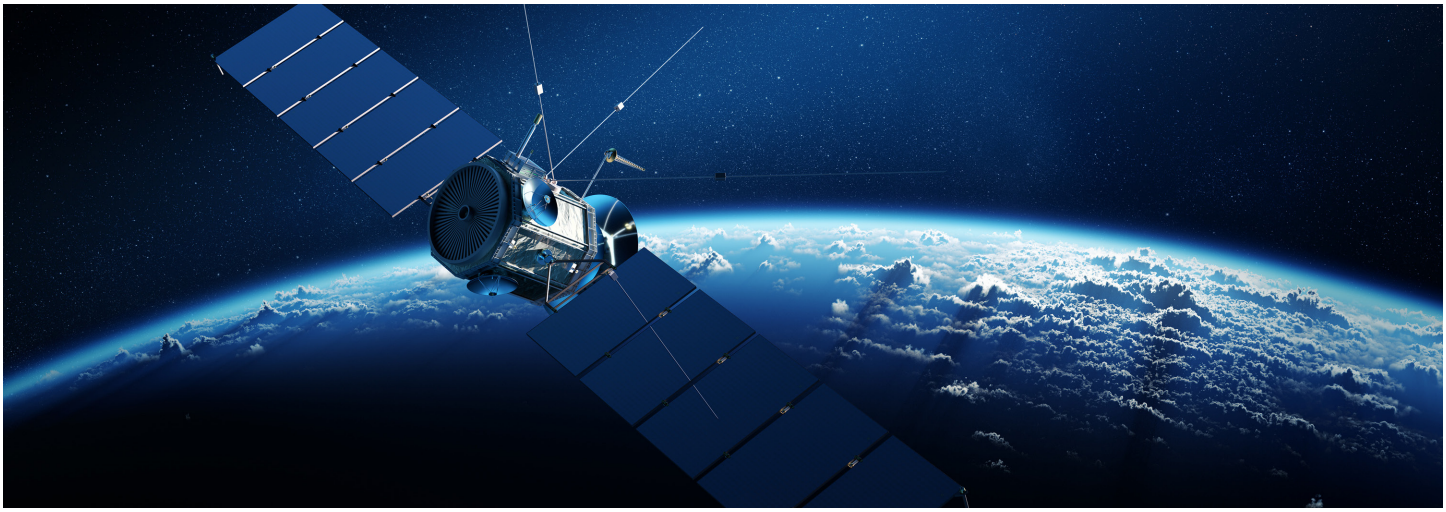
Mars Reconnaissance Orbiter



Curiosity (Mars Science Lab)

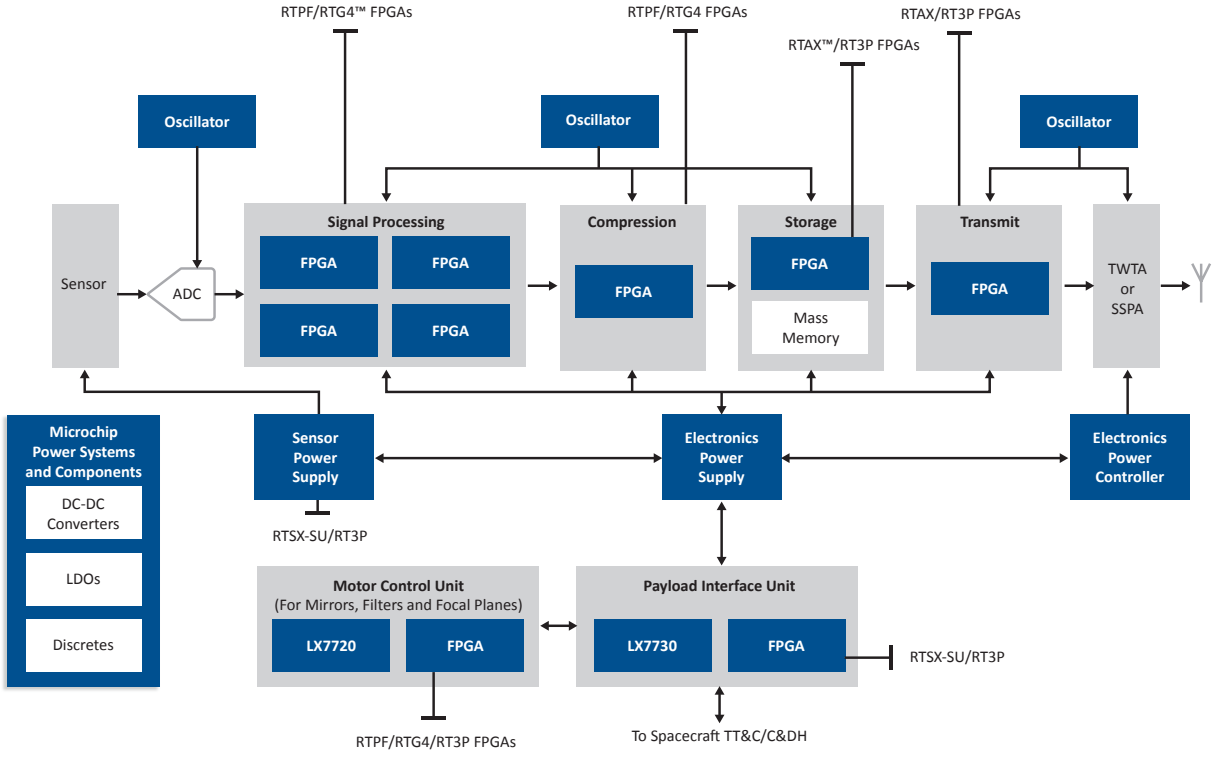
NASA IRIS

For more information, see https://www.microchip.com/en-us/products/fpgas-and-plds/radiation-tolerant-fpgas



Remote Sensing Payload Example

Our FPGAs have achieved flight heritage on many programs in command and control applications that require limited amounts of logic and modest performance levels. RT PolarFire® FPGAs have much greater logic density and much higher performance, which give significant improvements in signal processing throughput. Designers of high-speed data paths in space payloads can use RT PolarFire FPGAs to take advantage of the flexibility and ease of use of programmable logic. This is particularly important for remote sensing instruments, which must perform rapidly increasing amounts of on-board processing as sensor resolution is increasing faster than downlink bandwidth.



You can use RTSX-SU, RTAX and RT ProASIC 3 FPGAs for commanding, controlling and interfacing applications that require limited logic and performance. RT PolarFire and RTG4 FPGAs are well suited for situations that require maximum data throughput, such as signal processing and compression.

RT PolarFire FPGAs

Enabling New Capabilities for Space

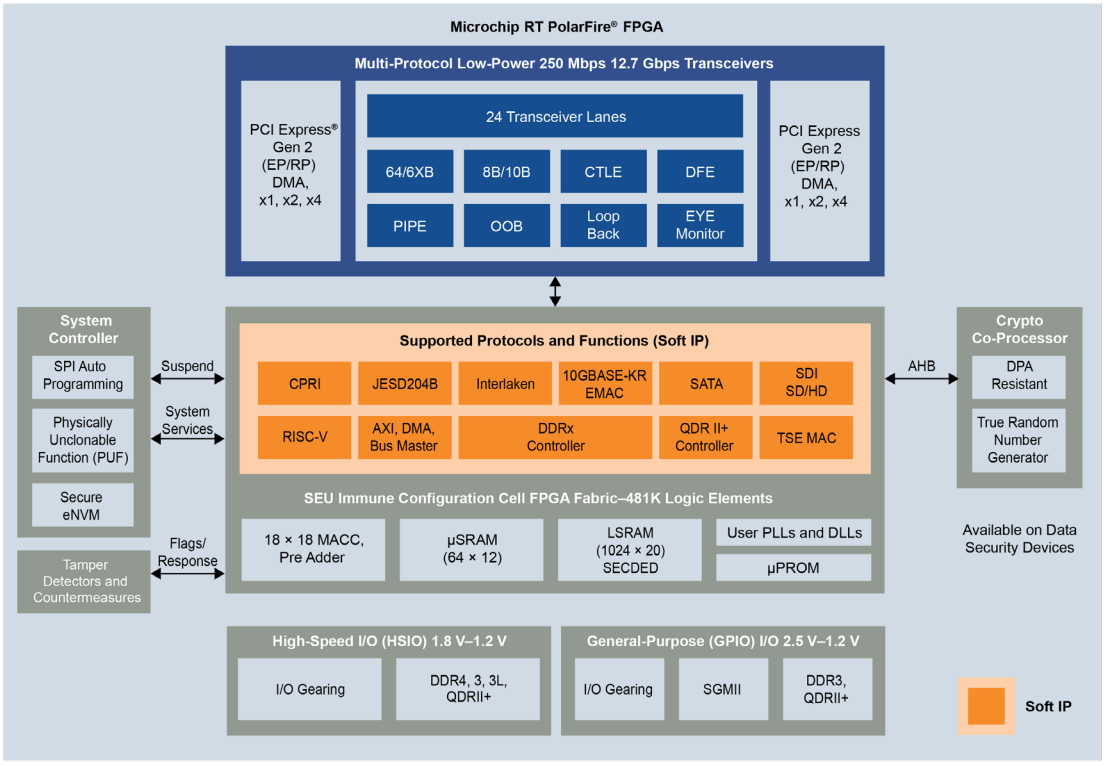
Features

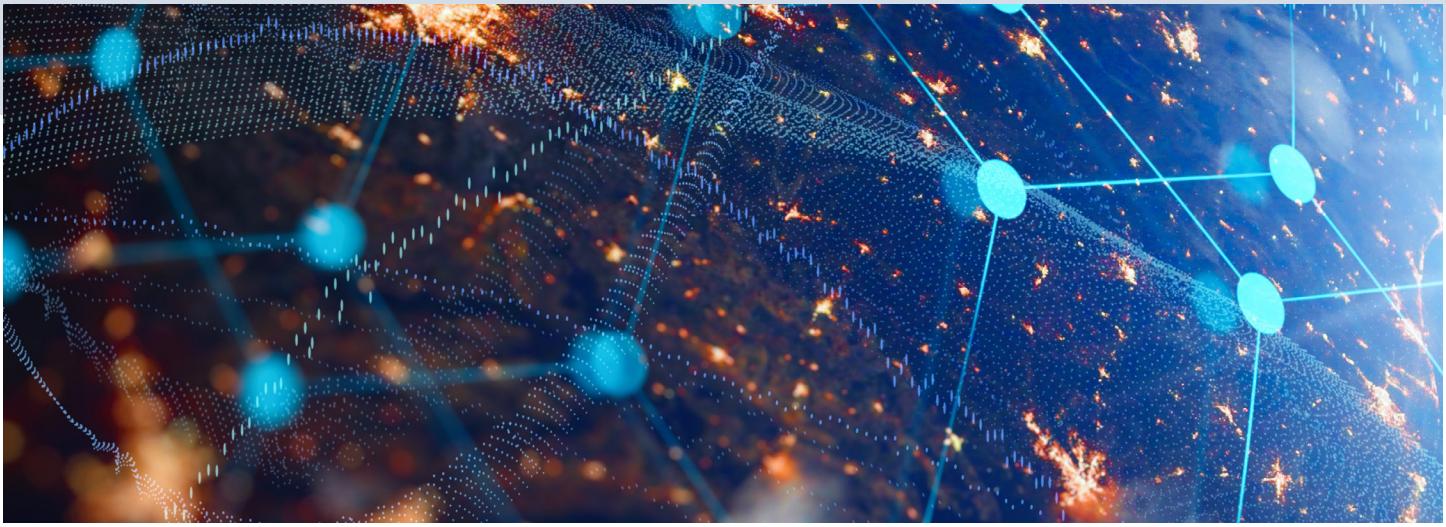
- Up to 481k LEs, 33 Mbits of memory and 1480 multipliers
- High-performance signal processing FPGA with 12.7-Gbps SerDes
- Lowest power consumption in class
- Path to QML V qualification

Advantages of Choosing a Microchip FPGA

- Technology that is immune to configuration upsets
- 60+ years of spaceflight heritage
- Expertise in radiation, quality and reliability
- Longstanding commitment to space

RT PolarFire FPGAs bring together our 60 years of spaceflight heritage and the industry's lowest-power PolarFire FPGA family to enable new capabilities for space applications. With 481,000 Logic Elements (LEs), 33 Mbits of embedded SRAM, 1,480 DSP blocks and 24 lanes of 10-Gbps transceivers, our next-generation radiation-tolerant FPGAs enable higher computing and connectivity throughout for mission-critical systems at 40% to 50% lower power than competing SRAM FPGAs while delivering greater immunity to configuration Single Event Upsets (SEUs).





Low Power and High Reliability

Like the award-winning PolarFire FPGA family, RT PolarFire FPGAs use low-power SONOS configuration switches embedded in a power-efficient architecture. The proof is in performance benchmarks that show PolarFire FPGAs providing a total power savings of 40% to 50% relative to comparable SRAM FPGAs. Resulting in a simpler and less expensive power supply design, the power savings achievable with RT PolarFire FPGAs translate to a major savings in cost of ownership and the reduced heat output results in simpler and less expensive thermal management.

For more information visit, https://www.microchip.com/en-us/products/fpgas-and-plds/radiation-tolerant-fpgas/rt-polarfire-fpgas

RT PolarFire FPGA Radiation Effects

We manufacture RT PolarFire FPGAs on a low-power 28-nm SONOS nonvolatile and reprogrammable PolarFire FPGA commercial die.

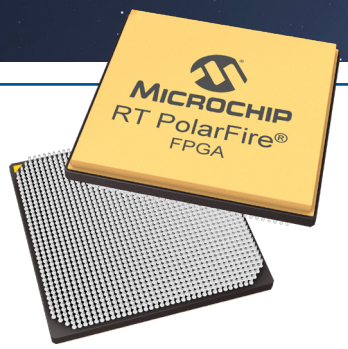
RT PolarFire FPGAs are immune to radiation (SEU)-induced changes in configuration due to the robustness of our SONOS cells used to connect and configure logic resources and routing tracks. The SynplifyPro synthesis tool, which is integrated into the available versions 12.0 and later of Libero® SoC Design Suite, can deploy soft TMR for LEs and flip-flops. RT PolarFire FPGAs support built-in Single Error Correction/Double Error Detection (SECDED) and memory interleaving.

Take advantage of the following benefits of RT PolarFire FPGAs:

- Total ionizing dose to >100 Krad (Si)
- Immunity to radiation-induced configuration upsets beyond 80 MeV-cm^2/mg
- Single-Event Latch-up (LET) threshold to LET_{TH} >60 MeV-cm2/mg (1.8V I/Os) and LET_{TH} 60 MeV-cm^2/mg (2.5V I/Os)
- SEU flip-flop upset rate with synthesized TMR <1.2×10^{-11} errors/bit-day (GEO solar min)
- SEU protection in fabric flip-flops that synthesis tools can instantiate
- Built-in SECDED and memory interleaving
- System controller suspend mode that protects against radiation SEUs

QML Class V Package Design

RT PolarFire FPGAs (RTPF500T) are 481,000-LE FPGAs that are available in hermetically sealed ceramic column grid array packages with 1,509 columns (Six Sigma 80Pb/20Sn) at 1.00-mm pitch. They feature integrated decoupling capacitors and they support qualification to QML class V.

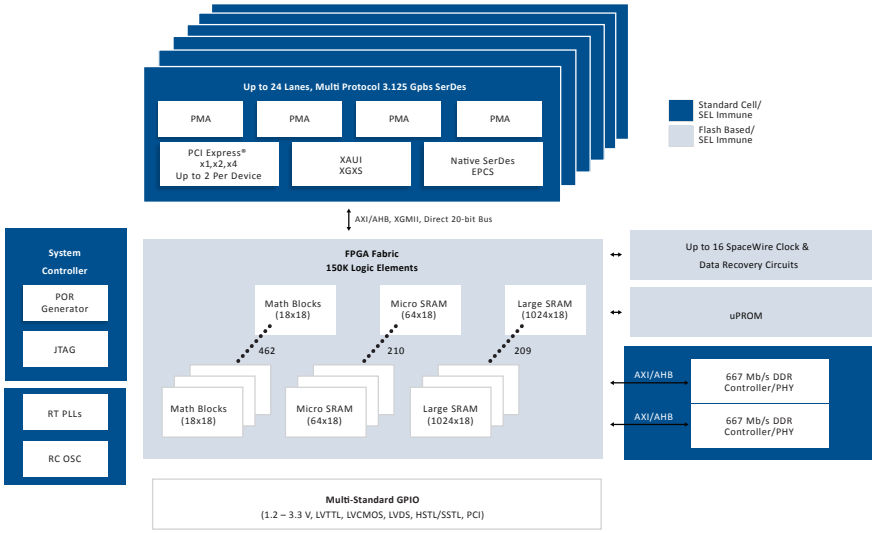


RT PolarFire FPGA Product Table

RT PolarFire® FPGAs	Features	RTPF500
FPGA Fabric	K Logic Elements (4 LUT + DFF)	481
	Math Blocks (18 × 18 MACC)	1480
	LSRAM Blocks (20 kb)	1520
	uSRAM Blocks (64 × 12)	4440
	Total RAM (Mb)	33
	uPROM (Kb 9-bit Bus)	513
	sNVM (KB)	56
	User DLLs/PLLs	8
High-Speed I/O	12.7-Gbps Transceiver Lanes	24
	PCIe® Gen 2 Endpoint Root Ports	2
Total I/Os	Total User I/Os	584
	HSIO	324
	GPIO	260
Packaging	CG/LG1509, 1.0-mm Pitch, 40-mm × 40-mm Size	1509

RTG4 FPGAs High-Speed QML Class V-Qualified FPGAs for Space

RTG4 FPGAs integrate our fourth-generation Flash-based FPGA fabric high-performance serialization/deserialization (SerDes) transceivers on a single chip while maintaining resistance to radiation-induced configuration upsets in the harshest radiation environments, such as Low Earth Orbit (LEO), Medium Earth Orbit (MEO), Geostationary Equatorial Orbit (GEO), Highly Elliptical Orbit (HEO) and deep space flight applications.



Key Benefits of RTG4 FPGAs

We manufacture RTG4 FPGAs using a low-power, 65-nm process with substantial reliability heritage. RTG4 FPGAs are immune to radiation (SEU)-induced changes in configuration due to the robustness of the Flash cells used to connect and configure logic resources and routing tracks. No background scrubbing or reconfiguration of the FPGA is needed to mitigate changes in configuration due to radiation effects.

Take advantage of the following features of these FPGAs:

- Total Ionizing Dose (TID) > 100 krad
- Configuration memory upsets immunity to LET > 103 MeV.cm2/mg
- Single-Event Latch-up (SEL) immunity to LET > 103 MeV.cm2/mg
- SEU-hardened registers that eliminate the need for Triple-Module Redundancy (TMR)
- SRAM with built-in Error Detection and Correction (EDAC)
- Global clocks and resets that are hardened against Single-Event Transients (SETs)

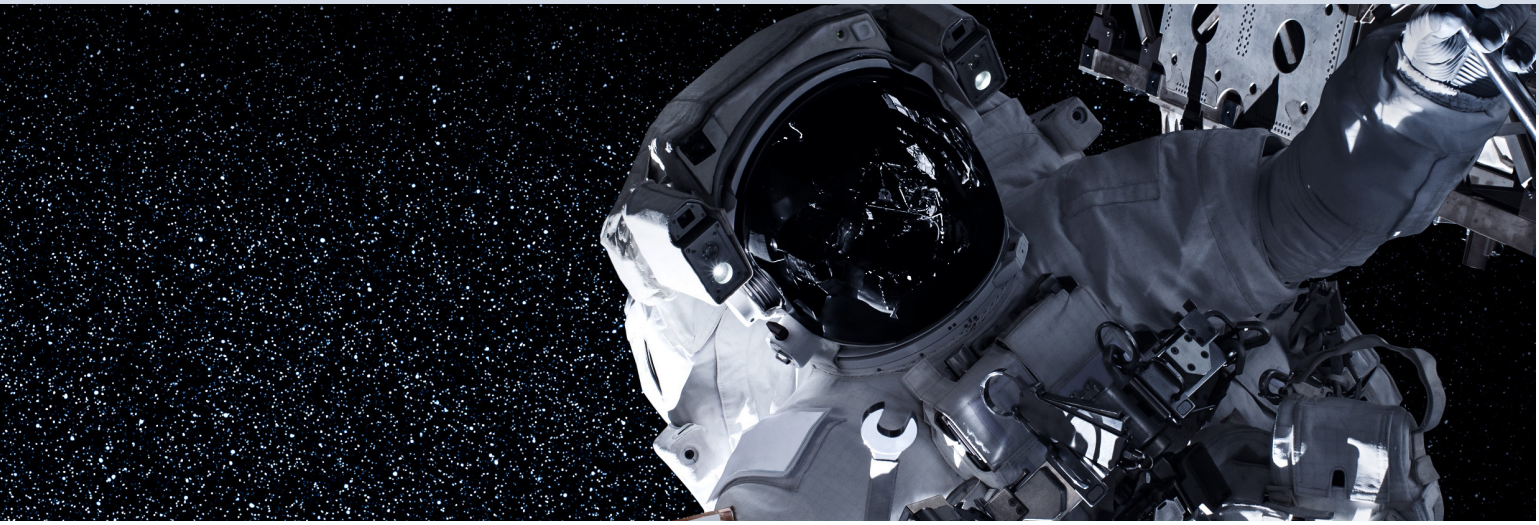
QML Class V qualification has been achieved for RTG4 FPGAs in CCGA/CLGA 1657 and CQFP 352 ceramic packages.

JEDEC qualification is completed for the FC/FCG 1657 sub-QML Ball Grid Array (BGA) plastic package, which is well suited for small satellite or constellation applications.

The RTG4 FPGA has achieved flight heritage on Mission Extension Vehicles (MEV) 1, 2, CAS-500, Landsat 9, Lucy, AIDA DART and is currently baselined in many US and international programs.

RTG4 FPGA Product Family

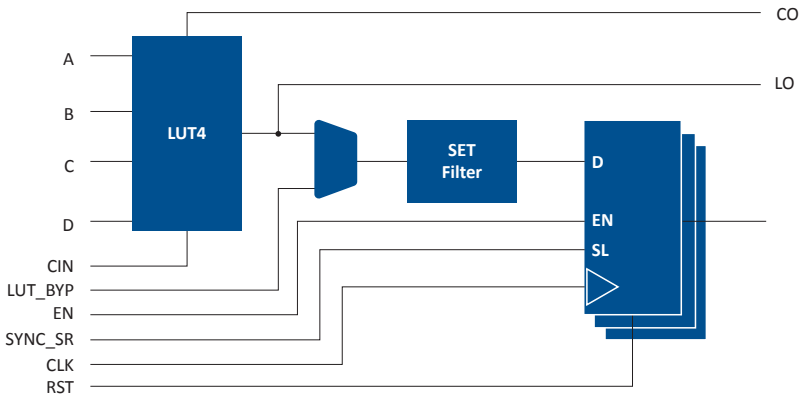
RTG4™ FPGA	RT4G150	Packages	
		CCGA/CLGA/FC/FCG 1657	CQ352
Logic/DSP	Maximum LEs (LUT4 + TMR flip-flop)	151, 824	151, 824
	Math blocks (18-bit × 18-bit)	462	462
	Radiation-tolerant PLLs	8	8
Memory	LSRAM 24.5 kbit blocks (with ECC)	209	209
	uSRAM 1.5 kbit blocks (with ECC)	210	210
	Total SRAM Mbits	5.2	5.2
	uPROM Kbits	374	374
High-Speed Interface	SerDes lanes (3.125 Gbps)	24	4
	PCIe® endpoints	2	1
	DDR2/3 SDRAM controllers (with ECC)	2	0
	SpaceWire clock and data recovery circuits	16	4
User I/Os	MSIO (3.3V)	240	166
	MSIOD (2.5V)	300	0
	DDRIO (2.5V)	180	0
	User I/O (excluding SerDes)	720	166



Logic Module

Dedicated STMR flip-flop with asynchronous self correction

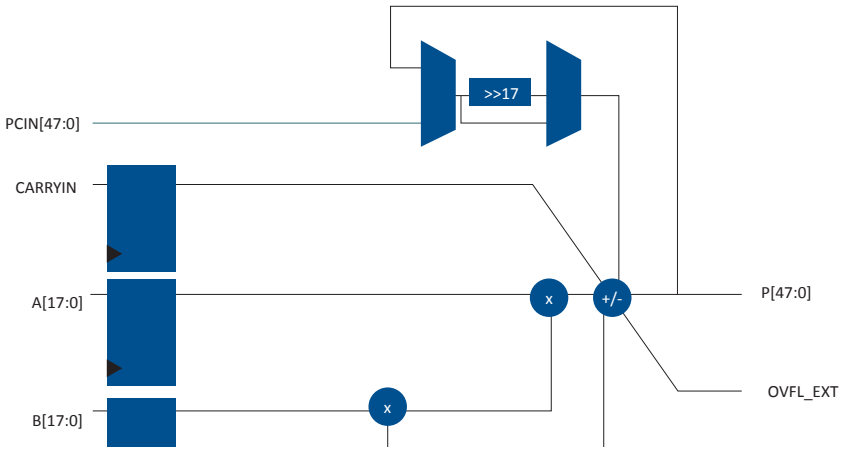
- With enable, global asynchronous set/reset and local synchronous set/reset
- Fast carry chain to complement math block performance
- 300 MHz for 32-bit functions (no SET filter)
- 250 MHz for 32-bit function (SET filter deployed)
- Industry-standard LUT4 for efficient synthesis
- LUT4 and flip-flop in same module can be used independently
- Hierarchical routing architecture enables >95% module utilization



Math Block

18 × 18 multiplier with advanced accumulate

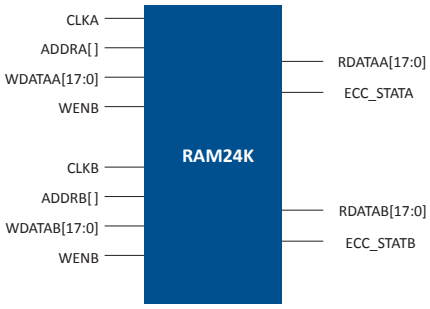
- High performance for signal processing throughput
- 300 MHz without SET mitigation
- 250 MHz with SET mitigation
- New 3-input adder function: (C + D) ± (A * B)
- Optional SEU-protected registers on inputs and outputs (including C input)

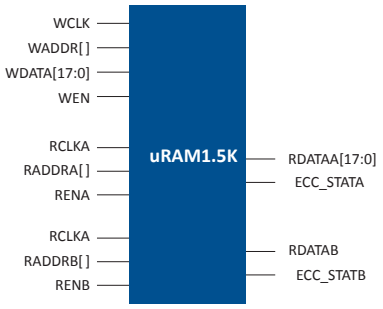


Memory Blocks

Radiation-tolerant built-in optional EDAC (SECDED)

- Resistant to multi-bit upset
- LSRAM up to 24.5 KBit
- Dual-port and two-port option
- High-performance synchronous operation
- Example usage—large FFT memory
- uRAM up to 1.5 KBit
- Three port memory—synchronous write port, two asynchronous or synchronous read ports
- Example usage—folded FIR filters and FFT twiddle factors

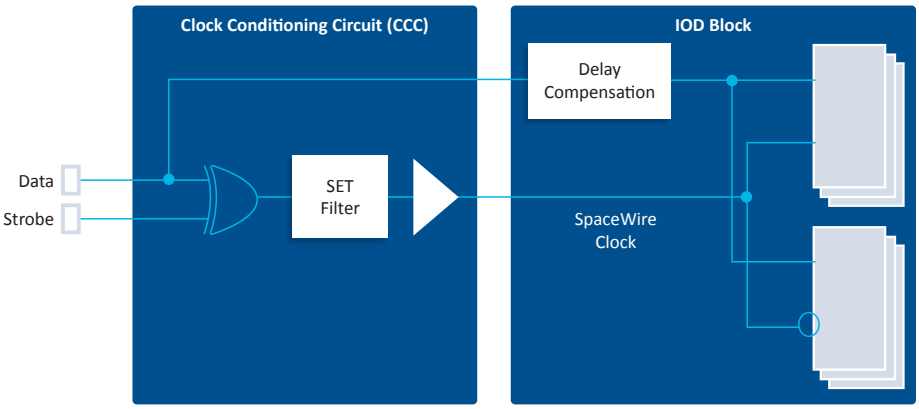




SpaceWire Receiver Interface

SpaceWire clock and data recovery

- Up to 16 hardwired clock and data recovery circuits
- Up to 200-Mbps SpaceWire data rate under optimum conditions
- Delay compensation for optimum alignment of clock and data
- Supports LVDS and LVTTL inputs



RTAX-S/SL FPGAs Radiation-Tolerant FPGA Alternative to Radiation-Hardened ASICs

RTAX-S/SL radiation-tolerant FPGAs offer industry-leading advantages for designers of spaceflight systems. Low-power consumption, true single-chip form factor and live-at-power-up operation all combine to make RTAX-S/SL devices the FPGAs of choice for space designers.

- Single Event Latch-Up (SEL) immune to LET_{TH} in excess of 117 MeV-cm^2/mg
- Single Event Upset less than $1E^{-10}$ errors per bit-day (worst-case geosynchronous orbit)
- Total Ionizing Dose (TID): 300 krad functional, 200 krad parametric
- Ceramic package offerings (CQFP, CCGA, CLGA)
- Prototype units with same footprint and timing as flight units
- Up to 840 user-programmable I/Os
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microchip Extended Flow
  V Flow: MIL-PRF-38535 QML Class V

RTAX-S/SL Devices

RTAX-S/SL Devices	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
Equivalent System Gates Capacity	250,000	1,000,000	2,000,000	4,000,000
Register (R-Cells) Modules	1,408	6,048	10,752	20,160
Combinatorial (C-Cells) Modules	2,816	12,096	21,504	40,320
Embedded RAM/FIFO Blocks (Without EDAC)	12	36	64	120
Embedded RAM/FIFO (Without EDAC) (k = 1,024 bits)	54k	162k	288k	540k
Hard-Wired Clocks (Segmentable)	4	4	4	4
Routed Clocks (Segmentable)	4	4	4	4
I/O Banks	8	8	8	8
User I/Os (Maximum)	248	418	684	840
I/O Registers	744	1,548	2,052	2,520
CG/LG Package Pins	624	624	624, 1152	1272
CQ Package Pins	208, 352	352	256, 352	352

I/Os per Package

RTAX-S/SL Devices	RTAX250S/SL				RTAX1000S/SL				RTAX2000S/SL				RTAX4000S/SL			
I/O Type	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os
CQ208	7	41	13	115												
CQ256									4	66	0	136				
CQ352	2	98	0	198	2	98	0	198	2	98	0	198	4	81	0	166
CG624	0	124	0	248	68	170	5	418	52	178	5	418				
CG1152									0	342	0	684				
CG1272													0	420	0	840

RTAX-DSP FPGAs Industry's Most Reliable Spaceflight FPGAs With DSP Capabilities

RTAX-DSP spaceflight FPGAs add embedded radiation-tolerant, multiply-accumulate blocks to the tried-and-trusted industry-standard RTAX-S/SL product family. The result is a dramatic increase in device performance and utilization when implementing arithmetic functions (such as those encountered in DSP algorithms) without sacrificing reliability or radiation tolerance. RTAX-DSP FPGAs integrate complex DSP functions into a single device without any external components for code storage or multiple-chip implementations for radiation mitigation.

Features of RTAX-DSP FPGAs

- Highly reliable, nonvolatile antifuse technology
- 2,000,000 to 4,000,000 system gates
- Up to 120 DSP math blocks with 125-MHz 18 × 18 bit multiply-accumulate
- Up to 540 Kbits of embedded memory with optional EDAC protection
- Up to 166 user-programmable I/Os
- RTAX-DL version with low static power
- Total dose: 300 Krad (functional) and 200 Krad (parametric)
- SEU less than $1E^{-10}$ errors per bit-day (worst-case GEO)
- SEL immune to LET^{TH} in excess of 117 MeV-cm^2/mg
- Enhanced SET for R-cells: 0.12 events/RTAX2000D device/100 years at 120 MHz
- Advanced CQFP packaging for space applications
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microchip Extended Flow
  V Flow: MIL-PRF-38535 QML Class V

RTAX-DSP Devices

RTAX-DSP Devices	RTAX2000D/DL	RTAX4000D/DL
Equivalent System Gates Capacity	2,000,000	4,000,000
Register (R-Cells) Modules	9,856	18,480
Combinatorial (C-Cells) Modules	19,712	36,960
Embedded Multiply-Accumulate DSP Math Blocks	64	120
Embedded RAM/FIFO Blocks (Without EDAC)	64	120
Embedded RAM/FIFO (Without EDAC) (k=1,024 bits)	288k	540k
Hard-Wired Clocks (Segmentable)	4	4
Routed Clocks (Segmentable)	4	4
I/O Banks	8	8
User I/Os (Maximum)	166	166
I/O Registers	2,052	2,520
CQ Package Pins	352	352

RT ProASIC® 3 FPGAs Low-Power, Reprogrammable FPGAs for Space

Radiation-Tolerant (RT) ProASIC® 3 FPGAs are the first to offer designers of spaceflight hardware a radiation-tolerant, reprogrammable, nonvolatile logic integration vehicle. They are intended for low-power space applications requiring up to 3,000,000 system gates.

Features of RT ProASIC 3 FPGAs

- Ceramic column grid array with Six Sigma™ copper-wrapped lead-tin columns
- Supports single-voltage system operation
- TID: 25 krad to 30 krad with less than 10% propagation delay change at standard test dose rate; up to 40 krad at low-dose rate
- Up to 504 Kbits of true dual-port SRAM
- Live-At-Power-Up (LAPU) level 0 support
- In-System Programming (ISP) protected with industry-standard on-chip 128-bit advanced encryption
- Standard (AES) decryption via JTAG (IEEE® 1532–compliant)
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microchip Extended Flow

RT ProASIC 3 FPGA Devices

RT ProASIC 3 FPGA Devices	RT3PE600L	RT3PE3000L
System Gates	600,000	3,000,000
VersaTiles (D-Flip-Flops)	13,824	75,264
RAM (k = 1,024 bits)	108k	504k
RAM Blocks (4,608 bits)	24	112
FlashROM (Kbits)	1	1
Secure (AES) ISP	Yes	Yes
Integrated PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
CG/LG Package Pins	484	484,896
CQ Package Pins	256	256

I/Os per Package

RT ProASIC 3 FPGA Devices	RT3PE600L		RT3PE3000L	
I/O Type	Single-Ended I/Os	Differential I/O Pairs	Single-Ended I/Os	Differential I/O Pairs
CG/LG484	270	135	341	168
CG/LG896	–	–	620	310
CQ256	166	82	166	82

RTSX-SU FPGAs Flight-Proven in Space—Time After Time

RTSX-SU radiation-tolerant FPGAs are enhanced versions of our commercial SX-A family of devices and we specifically designed them for enhanced radiation performance. Featuring SEU-hardened D-type flip-flops that offer the benefits of Triple Module Redundancy (TMR) without requiring cumbersome user intervention, the RTSX-SU family is a unique product for space applications.

- Very low power consumption (up to 68 µW at standby)
- 3.3V and 5.0V mixed voltage
- Configurable I/O support for 3.3V/5V PCI, LVTTL, TTL and CMOS
- Secure programming technology that protects against reverse engineering and design theft
- 100% circuit resource utilization with 100% pin locking
- Unique in-system diagnostic and verification capability with Silicon Explorer II
- Low-cost prototyping option
- Deterministic, user-controllable timing
- JTAG boundary scan testing in compliance with IEEE Standard 1149.1—dedicated JTAG reset (TRST) pin
- Highly reliable, nonvolatile antifuse technology
- 32,000 to 72,000 ASIC gates (48,000 to 108,000 system gates)
- Up to 360 user-programmable I/Os
- Hermetically sealed packages for space applications (CQFP, CCGA/CLGA, CCLG)

RTSX-SU Devices

I/Os per Package

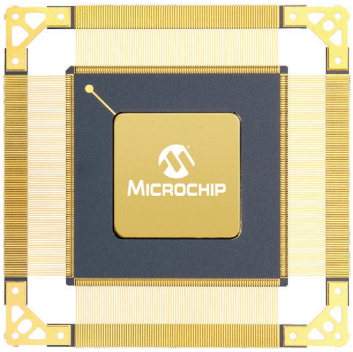
RTSX-SU Devices	RTSX32SU	RTSX72SU
CQ84	62	
CQ208	173	170
CQ256	227	212
CC256	202	

RTSX-SU Devices	RTSX32SU	RTSX72SU
Typical Gates Capacity	32,000	72,000
System Gates Capacity	48,000	108,000
Combinatorial Cells Logic Module	1,800	4,024
SEU-Hardened Register Cells (D-Flip-Flops) Logic Module	1,080	2,012
Maximum Flip-Flops Logic Module	1,980	4,024
Maximum User I/Os Logic Module	227	360
Clocks Logic Module	3	3
Quadrant Clocks Logic Module	0	4
Speed Grades Logic Module	Std., –1	Std., –1
CQ Package Pins	84, 208, 256	208, 256
CG Package Pins		624
CC Package Pins	256	

CG624	–	360

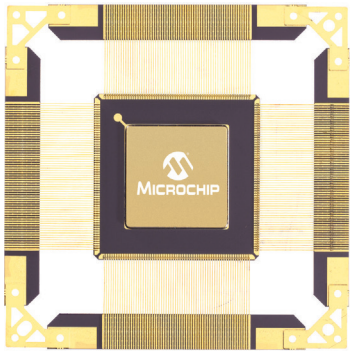
Note: The user I/Os include clock buffers.

FPGA Packages



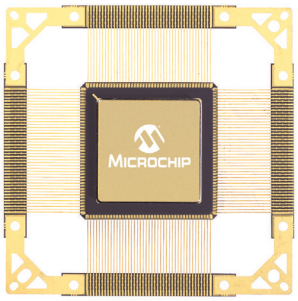
CQ352

b.s. 1.890" × 1.890" (48 mm × 48 mm)
h. RTAX FPGAs—105 mils (2.67 mm)
h. RTG4 FPGAs—89 mils (2.25 mm)
p. 20 mils (0.50 mm)



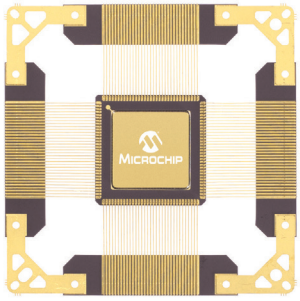
CQ256

b.s. 1.417" × 1.417" (36 mm × 36 mm)
h. 105 mils (2.67 mm)
p. 20 mils (0.50 mm)



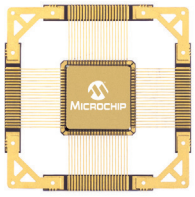
CQ172

b.s. 1.18" × 1.18" (29.972 mm × 29.972 mm)
h. 105 mils (2.67 mm)
p. 25 mils (0.64 mm)



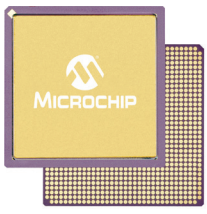
CQ132

b.s. 0.95" × 0.95" (24.13 mm × 24.13 mm)
h. 105 mils (2.67 mm)
p. 25 mils (0.64 mm)



CQ84

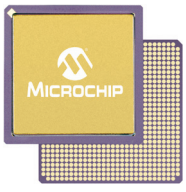
b.s. 0.65" × 0.65" (16.51 mm × 16.51 mm)
h. 90 mils (2.29 mm)
p. 25 mils (0.64 mm)



CG1152/LG1152

RTAX2000S and RTAX2000SL only

b.s. 1.378" × 1.378" (35 mm x 35 mm)
h. CCGA—218 mils (5.535 mm)
h. LGA—129 mils (3.28 mm)
p. 39 mils (1.00 mm)



CG896/LG896

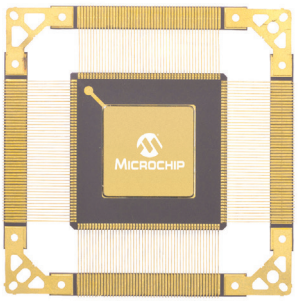
b.s. 1.220" × 1.220" (31 mm × 31 mm
h. CCGA—218 mils (5.535 mm)
h. LGA—129 mils (3.28 mm)
p. 39 mils (1.00 mm)

Note: b.s. is nominal package body size excluding leads, h is package thickness and p is pin/ball pitch.

FPGA Packages

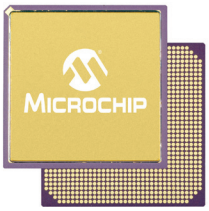
CQ208

b.s. 1.15" × 1.15" (29.21 mm × 29.21 mm)
h. 105 mils (2.67 mm)
p. 20 mils (0.50 mm)



CQ196

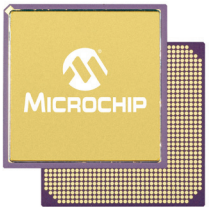
b.s. 1.35" × 1.35" (34.29 mm × 34.29 mm)
h. 105 mils (2.67 mm)
p. 25 mils (0.64 mm)



CB1657/CG1657/LG1657 /FC1657/FCG1657

RT4G150

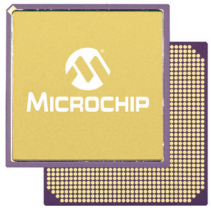
b.s. 1.693" × 1.693" (43 mm × 43 mm)
h. CBGA/FC/FCG—156 mils (3.97 mm)
h. CCGA—213 mils (5.42 mm)
h. CLGA—126 mils (3.21 mm)
p. 39 mils (1.00 mm)



CG1272/LG1272

RTAX4000S, RTAX4000SL, only

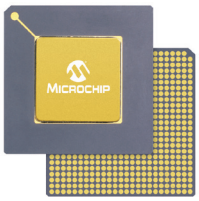
b.s. 1.457" × 1.457" (37 mm × 37 mm)
h. CCGA—218 mils (5.535 mm)
h. CLGA—129 mils (3.28 mm)
h. CLGA—126 mils (3.21 mm)
p. 39 mils (1.00 mm)



CG1509/LG1509

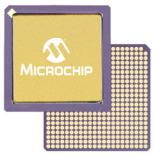
RTPF500

b.s. 1.575" × 1.575" (40 mm × 40mm)
h. CCGA- 276 mils (7.02 mm)
h. CLGA- 189.4 mils (4.81 mm)
p. 39 mils (1.00 mm)



CG624/LG624

b.s. 1.27" × 1.27" (32.50 mm × 32.50 mm)
h. CCGA—194 mils (4.94 mm)
h. LGA—90 mils (2.30 mm)
p. 50 mils (1.27 mm)



CG484/LG484

b.s. 0.91" × 0.91" (23.00 mm × 23.00 mm)
h. CCGA—225 mils (5.72 mm)
h. LGA—138 mils (3.51 mm)
p. 7.5 mils (0.19 mm)

CC256

b.s. 0.67" × 0.67" (17 mm × 17 mm)
h. 72 mils (1.847 mm)
p. 7.5 mils (0.19 mm)

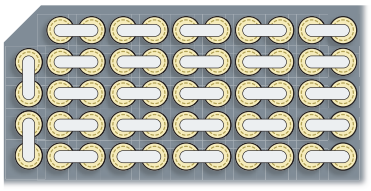
Note: b.s. is nominal package body size excluding leads, h is package thickness and p is pin/ball pitch.

Prototyping Solutions and Programming

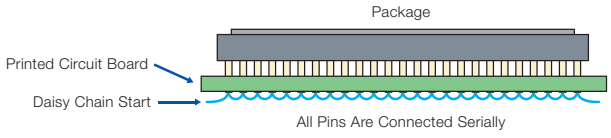
Daisy-Chained Packages

To facilitate the qualification of a target FPGA device socket and board assembly practices without using costly flight-quality parts, we offer certain Ceramic Column Grid Array (CCGA) and Ceramic Land Grid Array (CLGA) packages with adjacent pairs of pins tied together. By assembling these packages onto a qualification PC board that is laid out with adjacent pairs of solder pads tied together but offset by one pin as compared to the package, a single signal can be fed into one pin of the package and routed into and out of the entire package in a serial daisy chain fashion so that all pins of the package are used. This is useful for performing continuity and impedance tests to validate board assembly techniques with surface-mount grid array packages. Our daisy chain packages feature metal routing tracks between adjacent pairs of package pins within the package. For package qualification, an unbonded silicon die is included in the package.

Microchip Part Number	Mechanical Package
LG624_DAISY_CHAIN-1	624-pin CLGA
LG1152_DAISY_CHAIN	1152-pin CLGA
LG1272_DAISY_CHAIN	1272-pin CLGA
LG1657_DAISY_CHAIN	1657-pin CLGA
CG484_DAISY_CHAIN	484-pin CCGA
CG624_DAISY_CHAIN_SIX	624-pin CCGA
CG896_DAISY_CHAIN	896-pin CCGA
CG1152_DAISY_CHAIN	1152-pin CCGA
CG1272_DAISY_CHAIN	1272-pin CCGA
CG1657_DAISY_CHAIN	1657-pin CCGA
LG1509_DAISY_CHAIN	1509-pin CLGA
CG1509_DAISY_CHAIN	1509-pin CCGA



Partial View of 624 CGA With Adjacent Pin Pairs Tied Together



Programming Solutions

Silicon Sculptor 4

The Silicon Sculptor 4 programmer, which supports both antifuse and Flash FPGAs, delivers high data throughput and promotes ease of use while lowering the overall cost of ownership. The Silicon Sculptor 4 programmer includes a high-speed USB 2.0 interface that enables customers to connect multiple programmers to a single PC. This allows you to dynamically assemble an easily expandable, low- to medium-volume production programming system. Through the use of universal Microchip socket adapters, the Silicon Sculptor 4 programs Microchip packages, including PLCC, PQFP, VQFP, TQFP, QFN, PBGA, FBGA, CSP, CPGA, CQFP, CCGA and CLGA.

FlashPro 4/5/6

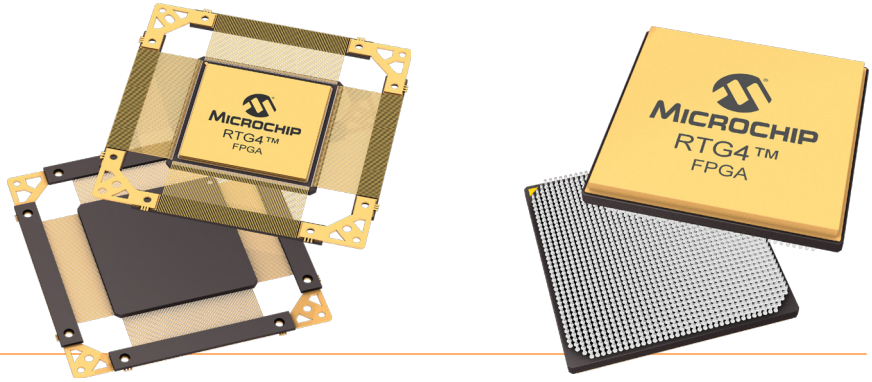
The FlashPro 4/5/6 programmers for Flash FPGAs utilize a JTAG interface, where a single JTAG chain can be used for multiple Flash devices on a JTAG chain. In-system programming using the JTAG port adds the flexibility of field upgrades or post-assembly production-line characterization. The elimination of expensive sockets on the board results in significantly reduced production costs.

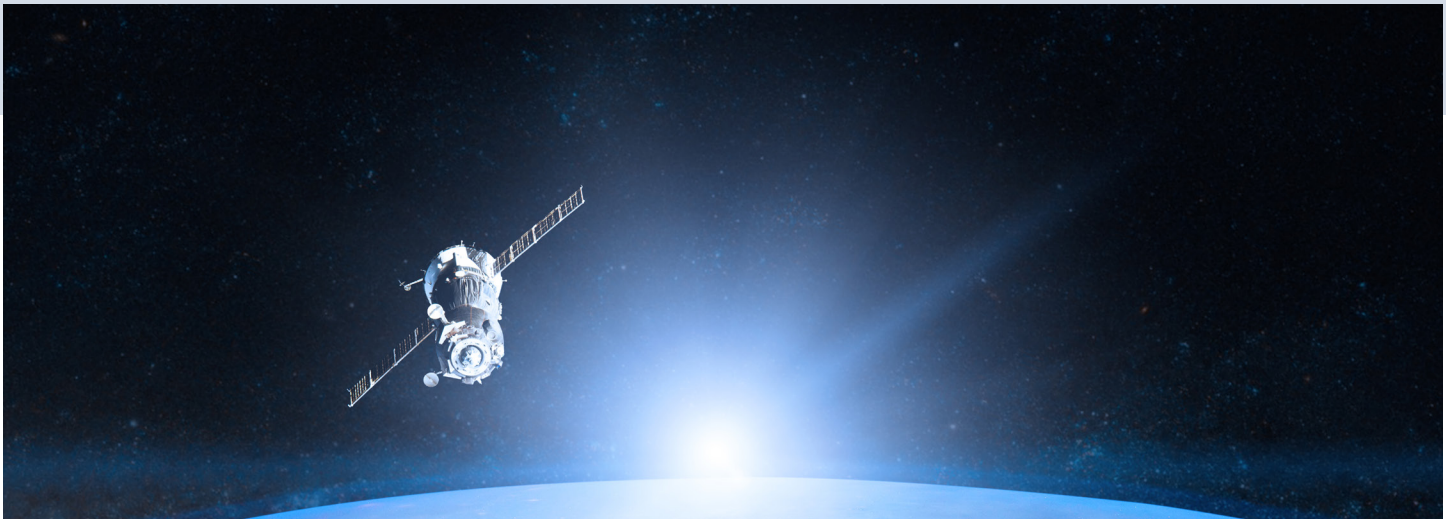
All FlashPro programmers use JEDEC-standard STAPL files, which means there are no algorithms built into the software. The FlashPro software and user interface support FlashPro4, and FlashPro5 programmers, eliminating the need to learn new software to switch from one hardware programmer to another.

https://www.microsemi.com/product-directory/programming-and-debug/4980-embedded-programming#overview

Prototyping With RTG4 FPGA PROTO Units

RTG4 PROTO FPGAs offer a development and prototyping solution for development and final timing validation of the flight design. As the RTG4 FPGA PROTO units use the same reprogrammable Flash technology as the flight units, the PROTO devices can be reprogrammed many times without removing them from the development board. The RTG4 FPGA PROTO prototype units have the same timing attributes as the RTG4 FPGA flight units, including support for the same speed grades as the flight parts. The RT-PROTO units are electrically tested in a manner to perform over the full military temperature range. Prototype units are offered in non-hermetic, ceramic packages. The prototype units include PROTO in their part number and PROTO is marked on devices to indicate that they are not intended for space flight. They are also not intended for applications that require the quality of spaceflight units, such as qualification of spaceflight hardware. RT-PROTO units offer no guarantee of hermeticity and no Mil-STD-883 class B processing. At a minimum, you should plan on using class B devices for all qualification activities.

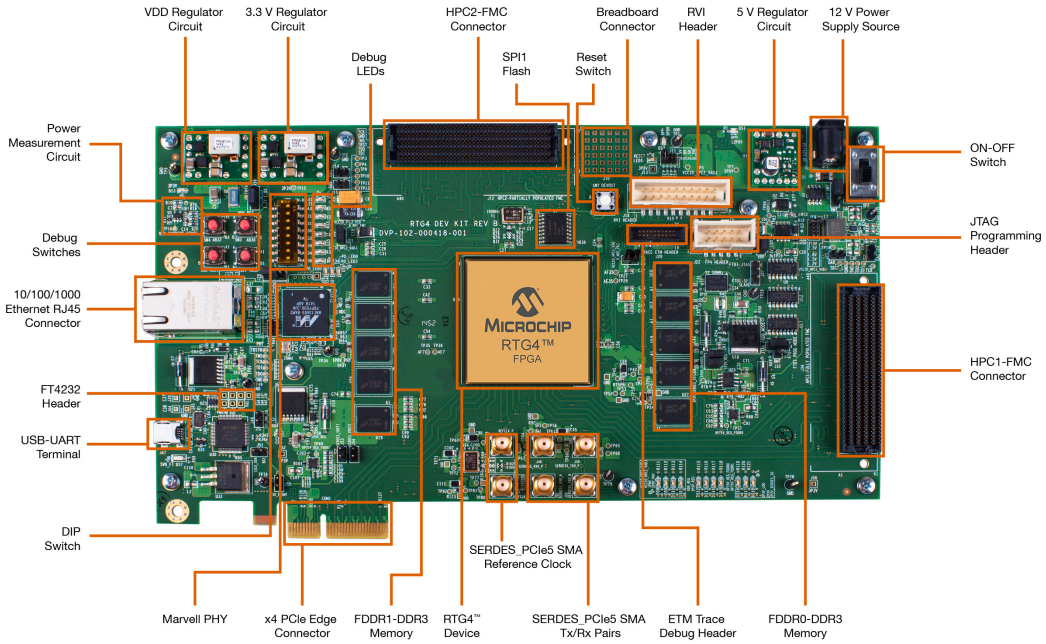




RTG4 FPGA Development Kit

The RTG4 FPGA Development Kit is an evaluation and development platform for applications such as data transmission, serial connectivity, bus interfaces and high-speed designs that use our latest radiation-tolerant, high-density, high-performance RTG4 FPGA family. The development board features an RT4G150 device offering more than 150,000 LEs in a ceramic package with 1,657 pins.

Part Number	Description
RTG4-DEV-KIT	RTG4 Development Board with one standard-speed RT4G150 PROTO device in 1657-pin, Ceramic Ball Grid Array (CBGA) package
RTG4-DEV-KIT-1	RTG4 Development Kit Board with one dash-1 speed (15% faster than standard speed) RT4G150 PROTO device in 1657-pin Ceramic Ball Grid Array (CBGA) package
RTG4-DEV-KIT-CG	RTG4 Development Board with one standard-speed RT4G150PROTO device in 1657-pin, Ceramic Column Grid Array (CCGA) package
RTG4-DEV-KIT-CG-1	RTG4 Development Board with one dash-1 speed (15% faster than standard speed) RT4G150 PROTO device in 1657-pin Ceramic Column Grid Array (CCGA) package

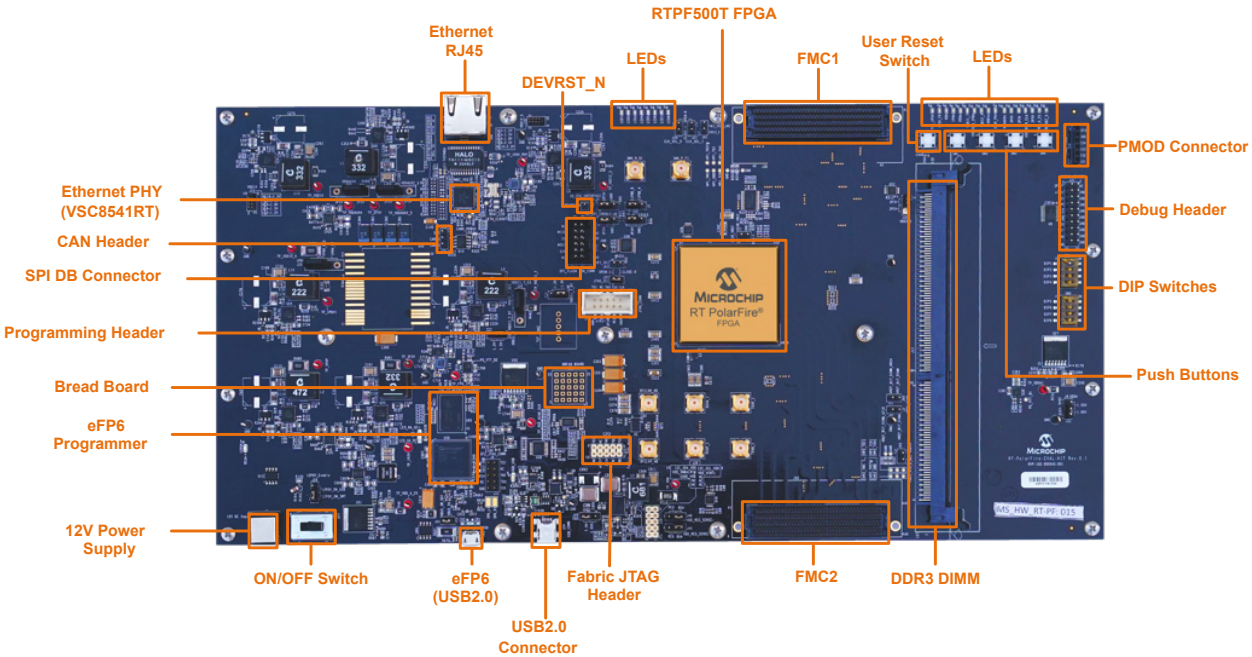


RT PolarFire FPGA Development Kit

RT PolarFire FPGA development kit provides a platform to customers for developing and evaluating Control, DSP, AI/ML, and Image Processing applications along with high speed serial connectivity and bus interfaces using Microchip's latest radiation tolerant RT PolarFire FPGAs.

Ordering Information

Part Number	Description
RTPF-DEV-KIT-CB	RT PolarFire Development Kit with one standard speed grade RTPF500T PROTO device in 1509-pin, Ceramic Ball Grid Array (CBGA) package
RTPF-DEV-KIT-CB-1	RT PolarFire Development Kit with one "-1" speed grade (15% faster than standard speed) RTPF500T PROTO device in 1509-pin, Ceramic Ball Grid Array (CBGA) package
RTPF-DEV-KIT-CG	RT PolarFire Development Kit with one standard speed grade RTPF500T PROTO device in 1509-pin, Ceramic Column Grid Array (CCGA) package
RTPF-DEV-KIT-CG-1	RT PolarFire Development Kit with one "-1" speed grade (15% faster than standard speed) RTPF500T PROTO device in 1509-pin, Ceramic Column Grid Array (CCGA) package



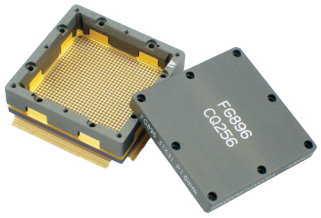
Package Prototyping Solutions

We've developed multiple low-cost prototyping solutions for RTAX-S/SL devices that ultimately are packaged in CQFP or CCGA for the production system. These solutions utilize the Axcelerator family Fine Pitch Ball Grid Array (FBGA) or Ceramic Land Grid Array (CLGA) packages as prototyping vehicles:

- CQFP to FPGA adapter socket
- CQFP to CLGA adapter socket
- CCGA to FBGA adapter socket
- CCGA to CLGA adapter socket

The CQFP to FBGA adapter sockets have an FBGA configuration on the top and a CQFP configuration on the bottom. The adapter sockets enable customers to use a commercial Axcelerator FG package during prototyping, then switch to an equivalent CQ256 or CQ352 package for production.

Adapter Socket	Ordering Part Number	Prototyped and Prototype Device
CQ352 to FG484	SK-AX250-CQ352RTFG484S	For prototyping RTAX250S/ L-CQ352 or AX250-CQ352 using AX250-FG484 package
CQ352 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CQ352-KITBTM	For prototyping RTAX1000S/ L-CQ352 or AX1000-CQ352 using AX1000-FG896 package
CQ352 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CQ352-KITBTM	For prototyping RTAX2000S/ L-CQ352 or AX2000-CQ352 using AX2000-FG896 package
CQ256 to FG896	SH-AX2-CQ256-KITTOP and SK-AX2-CQ256-KITBTM	For prototyping RTAX2000S/ L-CQ352 or AX2000-CQ256 using AX2000-FG896 package
CG624 to FG484	SK-SX72-CG624RTFG484	For prototyping RTSX72SU-CG624 or A54SX72A-CG624 using A54SX72A-FG484 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	For prototyping RTAX1000S-CG624, RTAX1000SL-CG624, or AX1000-CG624 using AX1000-FG896 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	For prototyping RTAX2000S-CG624, RTAX2000SL-CG624, or AX2000-CG624 using AX2000-FG896 package



RTAX2000S CQ256 to FG896 Ceramic Adapter, Top and Bottom

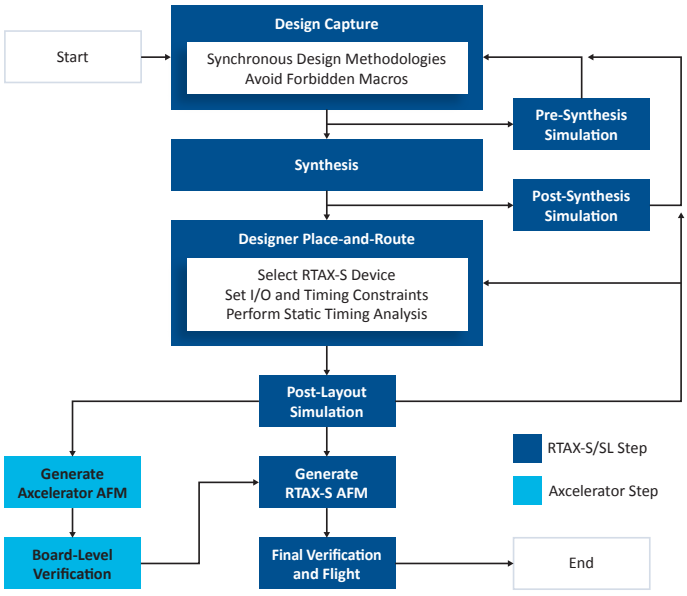
With the introduction of our RTAX-S/SL devices, you now have access to powerful FPGAs for aerospace and radiation-intensive applications. Prototype verification is an important step in system integration where accurate behavioral simulation and static timing analysis are crucial. Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, we have developed various prototyping options for RTAX-S/SL FPGAs for early design development and functional verification.

Prototyping With Axcelerator Units

The prototyping solution using the commercial Axcelerator devices consists of two parts.

- A well-documented design flow that allows the customer to target an RTAX-S/SL design to the equivalent commercial Axcelerator device
- A set of extender circuit boards that map the commercial device package to the appropriate RTAX-S/SL package footprint

This methodology provides the user with a cost-effective solution while maintaining the short time to market associated with our FPGAs.



Prototyping With RTAX-S/SL/DSP or RTSX-SU PROTO Units

The RTAX-S/SL/DSP or RTSX-SU PROTO units offer a prototyping solution that can be used for final timing verification of the flight design. The RTAX-S/SL/DSP or RTSX-SU PROTO prototype units have the same timing attributes as the RTAX-S/SL/DSP or RTSX-SU flight units. We offer prototype units in non-hermetic ceramic packages. The prototype units include PROTO in their part number and PROTO is marked on devices to indicate that they are not intended for space flight. They also are not intended for applications that require the quality of spaceflight units, such as qualification of spaceflight hardware. RT-PROTO units offer no guarantee of hermeticity and no MIL-STD-883B processing. At a minimum, you should plan on using class B level devices for all qualification activities. The RT-PROTO units are electrically tested to perform over the full military temperature range. The RT-PROTO units will also be offered in –1 or standard speed grades to validate the timing attributes of space designs using actual flight silicon.

RTAX-S/SL Prototyping With Flash Devices

Aldec's RTAX-S/SL prototyping solution allows you to take advantage of Flash-based reprogrammable ProASIC 3 FPGA devices. Aldec provides software that remaps antifuse primitives to Flash, which reduces design time and cost. In addition, the hardware adapter is footprint compatible with RTAX-S/SL devices; therefore, you do not need to redesign a new board for prototyping.

Microchip Technology Inc. | 2355 W. Chandler Blvd. | Chandler AZ, 85224-6199 | microchip.com

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